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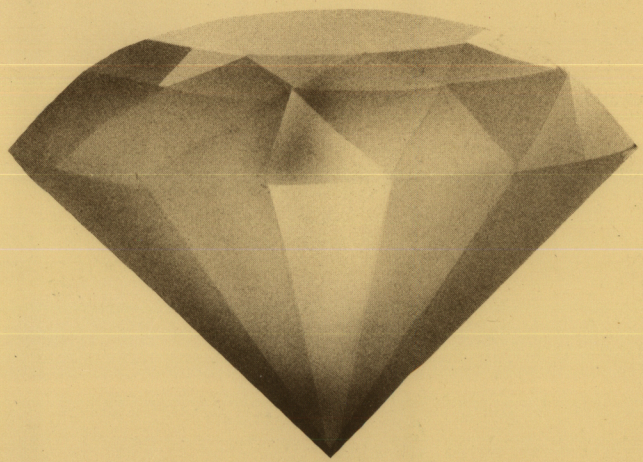

TOPAZ
SEMICONDUCTOR

CMOS/D-MOS ANALOG SWITCHES
D-MOS FETs

TOPAZ
SEMICONDUCTOR

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LIFE SUPPORT POLICY
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SECTION 1

TOPAZ SEMICONDUCTOR

Topaz Semiconductor Inc. was founded in March of 1985. The company specializes in design and manufacturing high performance devices for high frequency analog signal processing and medium power, high voltage transistors and smart power circuits. The technologies used are double-diffused MOS, (D-MOS) and D-MOS integrated with complementary MOS, (CMOS/D-MOS).

The D-MOS process can be utilized to reduce gate length (lateral D-MOS) or to increase transistor breakdown voltage (vertical D-MOS). Short gate length increases the speed of lateral D-MOS devices beyond that achievable with other silicon structures. Hence, lateral D-MOS FETs can provide a performance bridge between other silicon devices and GaAs devices. Lateral D-MOS devices are used extensively in applications ranging from large signal analog switching, (RF, video, ATE, telephone, etc.), to small signal VHF/VHF amplifiers, and high-speed digital interface applications, such as pin drivers in automatic test equipment and logic analyzer probes.

Depletion mode, (normally-ON), lateral D-MOS FETs can be substituted for J-FETs in many applications and extend high frequency performance by an order of magnitude.

Vertical D-MOS can operate at high voltages, over 600V, yet can be controlled by small amplitude, very low current signals. Topaz Semiconductor specializes in ultra low leakage, low threshold and multiple chip configurations used in back plane testers, signal analyzers, solid state relays and display driver applications.

Vertical D-MOS devices with gate-source standoff voltage above 100 volts are used as replacements for reed relays. Another application is high voltage switching without level shifting.

CMOS/D-MOS integrated circuits feature high off isolation at video frequencies combined with low insertion loss. The major applications are in video and RF switching. On chip control of high frequency signal switching reduces crosstalk between channels and increases the level of integration.

Topaz Semiconductor has a state-of-the-art, class 10, 5" wafer fabrication line located at its San Jose facility. The company's focus is on development of new, higher performance products within selected market segments, i.e., signal processing and smart power areas. The key element in this strategy is the utilization and further enhancement of D-MOS technology.

Topaz Semiconductor manufactures a large number of standard D-MOS and CMOS/D-MOS products. Some of the new products are designed to be compatible with existing industry standard devices. When used in place of those standard parts, they provide an economical way of extending performance of existing systems.

In addition to standard catalog parts, Topaz Semiconductor also manufactures application specific products, offers special processing and selections, and high reliability products tested to military requirements.

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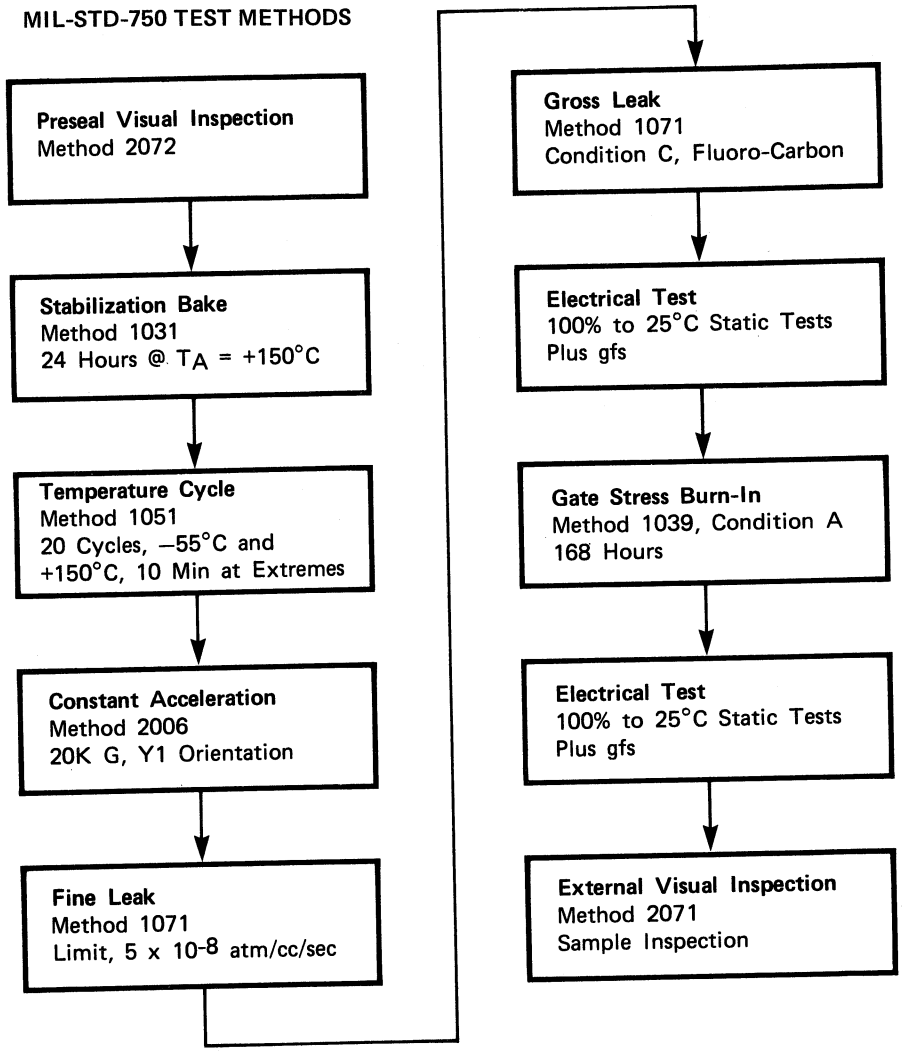
VN2410CHP	CHIP	D-MOS FET N-CHAN 240V 10 ohm	2-136
VN2410L	TO-92	D-MOS FET N-CHAN 240V 10 ohm	2-136
VP0104N3	TO-92	D-MOS FET P-CHAN -40V 8.0 ohm	2-139
VP0104ND	CHIP	D-MOS FET P-CHAN -40V 8.0 ohm	2-139
VP0106N3	TO-92	D-MOS FET P-CHAN -60V 8.0 ohm	2-139
VP0106ND	CHIP	D-MOS FET P-CHAN -60V 8.0 ohm	2-139
VP0109N3	TO-92	D-MOS FET P-CHAN -90V 8.0 ohm	2-139
VP0109ND	CHIP	D-MOS FET P-CHAN -90V 8.0 ohm	2-139
VP0808CHP	CHIP	D-MOS P-CHAN -80V 5.0 ohm	2-142
VP0808L	TO-92	D-MOS P-CHAN -80V 5.0 ohm	2-142
VP0808M	TO-237	D-MOS P-CHAN -80V 5.0 ohm	2-142
VP1008CHP	CHIP	D-MOS P-CHAN -100V 5.0 ohm	2-142
VP1008L	TO-92	D-MOS P-CHAN -100V 5.0 ohm	2-142
VP1008M	TO-237	D-MOS P-CHAN -100V 5.0 ohm	2-142
VQ1000J	14-PDIP	QUAD D-MOS FET N-CHAN 60V 5.5 ohm	2-145

SECTION 2

M+ PROCESS OPTION FLOW CHART



NOTES:

1. Device mark after seal and prior to first electrical test.
2. Applicable to TO-18, TO-39 and TO-72 hermetic packages.
3. Off Shore build, US test and Burn-In and QC inspection.
4. All devices are shipped with shorting rings on leads.
5. All devices are shipped in bulk, packed in anti-static bags.

ORDERING INFORMATION:

To order standard catalog parts with M+ Product Enhancement, add /M to standard part number. eg: SD215DE/M

N-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FETs

BV_{DSS} (Volts) MIN	$r_{DS(on)}$ (ohms) MAX	SINGLE TO-18 HERMETIC	SINGLE TO-39 HERMETIC	SINGLE TO-92 PLASTIC	SINGLE TO-237 PLASTIC	QUAD 14-Pin DIP PLASTIC	OCTAL 18-Pin DIP PLASTIC	FEATURES/ APPLICATIONS
600	60			SD1500BD				High BV_{DSS}
550				SD1501BD				Small Package
450	700	SD1200DD						Low Capacitance
	35	SD1100DD	SD1100HD					
400	500	SD1201DD						Low Capacitance
	350						AN0140NA	Low Leakage, I_{DSS} 5.0nA max for 8 channels
	25	SD1101DD	SD1101HD	SD1101BD				
300	300						AN0130NA	Low Leakage, I_{DSS} 5.0nA max for 8 channels
250	10	SD1102DD	SD1102HD	SD1102BD				
240	10			VN2410L				
200	300						AN0120NA	Low Leakage, I_{DSS} 5.0nA max for 8 channels
	250			SD1202BD				Low Leakage Low Capacitance
	28			SD1122BD				Reversed S-D Pin-Out Lead-Formed to TO-18
	10	SD1113DD	SD1113HD	SD1113BD				
	7.0	SD1112DD	SD1112HD	SD1112BD				
100	100						AN0110NA	Low Leakage, I_{DSS} 5.0nA max for 8 channels
	4.0	SD1107DD	SD1107HD	SD1107BD		SD1107N		
		SD1105DD	SD1105HD	SD1105BD				
	3.0	SD1104DD	SD1104HD	SD1104BD				
				TN0110N3				Low Threshold, V_T 1.5V max
	2.5		CF		CF			
	0.6		2N6782					
			SD3300HD	SD3300BD	SD3300AD			
90	3.0			VN0109N3				
80	4.0	SD1115DD	SD1115HD	SD1115BD				
	3.0	SD1114DD	SD1114HD	SD1114BD				
	2.5		CF		CF			

CF—Contact Factory

N-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FETs (CONTINUED)

BV_{DSS} (Volts) MIN	$r_{DS(on)}$ (ohms) MAX	SINGLE TO-18 HERMETIC	SINGLE TO-39 HERMETIC	SINGLE TO-92 PLASTIC	SINGLE TO-237 PLASTIC	QUAD 14-Pin DIP PLASTIC	OCTAL 18-Pin DIP PLASTIC	FEATURES/ APPLICATIONS
60	7.5			VN2222LL	VN2222LM			
	5.5					VQ1000J		
	5.0	SD1106DD		2N7000 SD1124BD VN0610LL VN10KN3	SD1106AD VN10LM			
	4.0			SD1127BD				Low Leakage, I_{DSS}1.0nA max
	3.0			TN0106N3				Low Threshold, V_T 1.5V max
				VN0106N3				
	2.5	SD1117DD	SD1117HD	SD1117BD	CF	SD1117N		
				SD1137BD				Low Threshold, V_T 1.5V max
	0.6		2N6781					
	0.4		SD3301HD	SD3301BD	SD3301AD			
40	3.0			VN0104N3				
	2.5				CF			

CF—Contact Factory

P-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FETs

BV_{DSS} (Volts) MIN	$r_{DS(on)}$ (ohms) MAX	SINGLE TO-18 HERMETIC	SINGLE TO-39 HERMETIC	SINGLE TO-92 PLASTIC	SINGLE TO-237 PLASTIC	QUAD 14-Pin DIP PLASTIC	OCTAL 18-Pin DIP PLASTIC	FEATURES/ APPLICATIONS
-400	700			SD2204BD			AP0140NA	
-300	600						AP0130NA	Low Leakage, I_{DSS}
-200	600						AP0120NA	-5NA max for 8 channels
-100	5.0	SD2107DD	SD2107HD	SD2107BD	SD2107AD	CF	CF	
				VP1008L	VP1008M			
-90	8.0			VP0109N3				
-80	5.0			VP0808L	VP0808M			
-60	8.0			VP0106N3				
-40	8.0			VP0104N3				

CF—Contact Factory

N-CHANNEL ENHANCEMENT-MODE LATERAL D-MOS FETs

BV_{DSX} (Volts) MIN	BV_{DSX} (Volts) MIN	$r_{DS(on)}$ (ohms) MAX	SINGLE TO-39 HERMETIC	SINGLE TO-52+ HERMETIC	SINGLE TO-72 HERMETIC	SINGLE TO-92 PLASTIC	DUAL TO-78 HERMETIC	QUAD 14/16-Pin DIP PLASTIC	QUAD SO-14 SURFACE MOUNT	SINGLE SOT-143 SURFACE MOUNT
60	0.5	9.0	SD220HD							
30	10	70			SD210DE					
					2N7104					
					SD211DE*					CF*
					2N7105*					
					SD211ADE*					
	0.5	80						SD5200N*		
		70						SD5100N*		
25	20	6.0			SD219DE*					
	15				SD217DE*					
	0.5	130			SD304DE*					
		70		SD200DC						
				SD201DC*						
		6.0	SD205HD*							
20	20	70			SD214DE					
					2N7108					
					SD215DE*			SD5000N*	SD5400CY*	CF*
					2N7109*					
					SD215ADE*					
	0.5	100			SD306DE*					
		80		SD303DC*						
		50		SD202DC						
				SD203DC*						
		20				TZ404BD*				
15	15	70						SD5002N*	SD5402CY*	
	0.5	80				TZ402BD*				
		70						SD5101N*		
		60				TZ403BD*				
10	10	70			SD212DE		SD411HD*			
					2N7106					
					SD213DE*			SD5001N*	SD5401CY*	CF*
					2N7107*					

*—Gate Protective Diode(s) +—4-Lead TO-52 Package CF—Contact Factory

N-CHANNEL DEPLETION-MODE LATERAL D-MOS FETs

BV_{DSX} (Volts) MIN	BV_{DSX} (Volts) MIN	$r_{DS(on)}$ (ohms) MAX	SINGLE TO-39 HERMETIC	SINGLE TO-52+ HERMETIC	SINGLE TO-72 HERMETIC	SINGLE TO-92 PLASTIC	DUAL TO-78 HERMETIC	QUAD 16-Pin DIP PLASTIC	
20	10	75			SD2200DE*				
		150			SD2100DE*		TZ5911HD*	SD5501N*	

VERTICAL and LATERAL D-MOS FET SUBSTITUTION GUIDE

NOTE: See separate listings for Analog Switch and Analog Multiplexer Substitution Guide and J-FET Replacement Guide.

LEGEND:

PART NO.	Manufacturer's part number, complete for ordering purposes.	
CHAN.	N-Channel, P-Channel or N+P Channel Arrays.	
DESCRP.	DEPL	— Depletion-mode (Normally On.). Unless otherwise stated, all devices are Enhancement-Mode (Normally Off).
	DG	— Dual Gate
	DUAL	— 2-Channel
	OCTAL	— 8-Channel
	QUAD	— 4-Channel
	SOT	— Small Outline Transistor Package.
	Z	— Gate Protective Diode(s).
BV_{DSS}	Drain-Source Breakdown Voltage.	
$I_{D(on)}$	ON Drain Current at T_C or T_A = +25° C.	
PACKAGE	CHIP	— Individual chips, usually in Waffle Pack.
	CDIP	— Ceramic Dual In-Line on Ceramic Side-Brazed Package.
	LF	— Lead Formed.
	SO-14	— Small Outline, 14-Pin Package.
	TO	— JEDEC Package.
	52+	— 4-Lead variation of TO-52 Package.
	92R	— Reversed Source and Drain Leads.
	143	— SOT-143, Small Outline 4-Pin Package.
TOPAZ PART NUMBER	CF	— Contact Factory for details on available alternative products.
	(Part No.)	— Functional equivalent in similar or identical package which nearly meets, equals, or exceeds key parameters of Part Number.

Amperex

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
BS170	N		60	5.000	0.19	92LF	SD1124BD
BST70A	N		80	4.000	0.50	92	SD1107BD
BST72A	N		100	10.000	0.30	92	SD1107BD

Ferranti

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
BS107P	N		200	23.000	0.12	92R	SD1122BD
BS107PT	N		200	28.000	0.12	92R	SD1122BD
BS170P	N		60	5.000	0.50	92R	SD1124BD
BS250P	P		-60	14.000	-.23	92	VP0106N3
VN10LP	N		60	5.000	0.27	92	VN10KN3
ZVN0104A	N		40	4.000	0.38	92	SD1107BD
ZVN0104B	N		40	4.000	0.86	39	SD1107HD
ZVN0104D	N		40	4.000	0.00	CHIP	SD1107CHP
ZVN0106A	N		60	4.000	0.32	92	SD1107BD
ZVN0106B	N		60	4.000	0.85	39	SD1107HD
ZVN0106D	N		60	4.000	0.00	CHIP	SD1107CHP
ZVN0108A	N		80	4.000	0.32	92	SD1107BD
ZVN0108B	N		80	4.000	0.85	39	SD1107HD
ZVN0108D	N		80	4.000	0.00	CHIP	SD1107CHP
ZVN0109A	N		90	4.000	0.38	92	SD1107BD
ZVN0109B	N		90	4.000	0.86	39	SD1107HD
ZVN0110A	N		100	8.000	0.26	92	SD1107BD
ZVN0110B	N		100	8.000	0.58	39	SD1107HD
ZVN0110D	N		100	8.000	0.00	CHIP	SD1107CHP
ZVN0114A	N		140	8.000	0.26	92	SD1112BD
ZVN0114B	N		140	8.000	0.58	39	SD1112HD
ZVN0114D	N		140	8.000	0.00	CHIP	SD1112CHP
ZVN0116A	N		160	16.000	0.18	92	SD1112BD
ZVN0116B	N		160	16.000	0.40	39	SD1112HD
ZVN0116D	N		160	16.000	0.00	CHIP	SD1112CHP
ZVN0117TA	N		170	23.000	0.16	92	SD1122BD
ZVN0120A	N		200	16.000	0.16	92	SD1112BD
ZVN0120B	N		200	16.000	0.42	39	SD1112HD
ZVN0120D	N		200	16.000	0.00	CHIP	SD1112CHP
ZVN0124A	N		240	16.000	0.16	92	SD1102BD
ZVN0124B	N		240	16.000	0.42	39	SD1102HD
ZVN01A2A	N		20	2.000	0.45	92	SD1117BD
ZVN01A2B	N		20	2.000	1.00	39	SD1117HD
ZVN01A2D	N		20	2.000	0.00	CHIP	SD1117CHP
ZVN01A3A	N		30	2.000	0.45	92	SD1117BD
ZVN01A3B	N		30	2.000	1.00	39	SD1117HD
ZVN01A3D	N		30	2.000	0.00	CHIP	SD1117CHP
ZVN0204B	N		40	2.000	1.32	39	SD1117HD
ZVN0204D	N		40	2.000	0.00	CHIP	SD1117CHP
ZVN0206B	N		60	2.000	1.32	39	SD1117HD
ZVN0206D	N		60	2.000	0.00	CHIP	SD1117CHP
ZVN0210B	N		100	4.000	0.90	39	SD1107HD
ZVN0210D	N		100	4.000	0.00	CHIP	SD1107CHP
ZVN0216B	N		160	8.000	0.64	39	SD1112HD
ZVN0216D	N		160	8.000	0.00	CHIP	SD1112CHP
ZVN0220B	N		200	8.000	0.64	39	SD1112HD
ZVN0220D	N		200	8.000	0.00	CHIP	SD1112CHP
ZVN02A2B	N		20	1.000	1.80	39	SD3301HD
ZVN02A2D	N		20	1.000	0.00	CHIP	SD3301CHP
ZVN02A3B	N		30	1.000	1.80	39	SD3301HD

Ferranti (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
ZVN02A3D	N		30	1.000	0.00	CHIP	SD3301CHP
ZVN0526A	N		260	40.000	0.10	92	SD1101BD
ZVN0530A	N		300	50.000	0.09	92	SD1101BD
ZVN0530B	N		300	50.000	0.15	39	SD1101HD
ZVN0530D	N		300	80.000	0.00	CHIP	SD1101CHP
ZVN0535A	N		350	50.000	0.09	92	SD1101BD
ZVN0535B	N		350	50.000	0.15	39	SD1101HD
ZVN0535D	N		350	80.000	0.00	CHIP	SD1101CHP
ZVN0540A	N		400	80.000	0.08	92	SD1101BD
ZVN0540B	N		400	80.000	0.17	39	SD1101HD
ZVN0540D	N		400	80.000	0.00	CHIP	SD1101CHP
ZVN0545B	N		450	80.000	0.17	39	SD1100HD
ZVN0545D	N		450	80.000	0.00	CHIP	SD1100CHP
ZVN1104B	N		40	1.000	1.90	39	SD3301HD
ZVN1104D	N		40	1.000	0.00	CHIP	SD3301CHP
ZVN1106B	N		60	1.000	1.90	39	SD3301HD
ZVN1106D	N		60	1.000	0.00	CHIP	SD3301CHP
ZVN1108B	N		80	1.000	1.90	39	SD3300HD
ZVN1108D	N		80	1.000	0.00	CHIP	SD3300CHP
ZVN1109B	N		90	1.000	1.90	39	SD3300HD
ZVN11A2B	N		20	0.500	2.50	39	SD3301HD
ZVN11A2D	N		20	0.500	0.00	CHIP	SD3301CHP
ZVN11A3B	N		30	0.500	2.50	39	SD3301HD
ZVN11A3D	N		30	0.500	0.00	CHIP	SD3301CHP
ZVN1204B	N		40	0.400	2.70	39	SD3301HD
ZVN1204D	N		40	0.400	0.00	CHIP	SD3301CHP
ZVN1206B	N		60	0.400	2.70	39	SD3301HD
ZVN1206D	N		60	0.400	0.00	CHIP	SD3301CHP
ZVN1210B	N		100	0.750	2.00	39	SD3300HD
ZVN1210D	N		100	0.750	0.00	CHIP	SD3300CHP
ZVN1304A	N		40	10.000	0.23	92	SD1107BD
ZVN1304B	N		40	10.000	0.52	39	SD1107HD
ZVN1304D	N		40	10.000	0.00	CHIP	SD1107CHP
ZVN1306A	N		60	10.000	0.20	92	SD1107BD
ZVN1306B	N		60	10.000	0.50	39	SD1107HD
ZVN1306D	N		60	10.000	0.00	CHIP	SD1107CHP
ZVN1308A	N		80	10.000	0.20	92	SD1107BD
ZVN1308B	N		80	10.000	0.50	39	SD1107HD
ZVN1308D	N		80	10.000	0.00	CHIP	SD1107CHP
ZVN1309A	N		90	10.000	0.23	92	SD1107BD
ZVN1309B	N		90	10.000	0.52	39	SD1107HD
ZVN1310A	N		100	20.000	0.16	92	SD1107BD
ZVN1310B	N		100	20.000	0.37	39	SD1107HD
ZVN1310D	N		100	20.000	0.00	CHIP	SD1107CHP
ZVN1314A	N		140	20.000	0.16	92	SD1113BD
ZVN1314B	N		140	20.000	0.37	39	SD1113HD
ZVN1314D	N		140	20.000	0.00	CHIP	SD1113CHP
ZVN1316A	N		160	40.000	0.12	92	SD1113BD
ZVN1316B	N		160	40.000	0.26	39	SD1113HD
ZVN1316D	N		160	40.000	0.00	CHIP	SD1113CHP
ZVN1320A	N		200	40.000	0.10	92	SD1113BD
ZVN1320B	N		200	40.000	0.25	39	SD1113HD
ZVN1320D	N		200	40.000	0.00	CHIP	SD1113CHP
ZVN1404A	N		40	250.000	0.01	92	SD1202BD
ZVN1404D	N		40	250.000	0.00	CHIP	SD1202CHP
ZVN1406A	N		60	250.000	0.01	92	SD1202BD
ZVN1406D	N		60	250.000	0.00	CHIP	SD1202CHP
ZVN1408A	N		80	250.000	0.01	92	SD1202BD
ZVN1408D	N		80	250.000	0.00	CHIP	SD1202CHP
ZVN1409A	N		90	250.000	0.01	92	SD1202BD

Ferranti (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
ZVN1410A	N		100	500.000	0.03	92	SD1202BD
ZVN1410D	N		100	500.000	0.00	CHIP	SD1202CHP
ZVN1414A	N		140	500.000	0.03	92	SD1202BD
ZVN1414D	N		140	500.000	0.00	CHIP	SD1202CHP
ZVN1416A	N		160	1000.000	0.02	92	SD1202BD
ZVN1416D	N		160	1000.000	0.00	CHIP	SD1202CHP
ZVN1420A	N		200	1000.000	0.02	92	SD1202BD
ZVN1420D	N		200	1000.000	0.00	CHIP	SD1202CHP
ZVN2104A	N		40	2.000	0.45	92	CF
ZVN2104B	N		40	2.000	1.20	39	CF
ZVN2106A	N		60	2.000	0.45	92	CF
ZVN2106B	N		60	2.000	1.20	39	CF
ZVN2110A	N		100	4.000	0.32	92	SD1107BD
ZVN2110B	N		100	4.000	0.85	39	SD1107HD
ZVN2115A	N		150	16.000	0.16	92	SD1113BD
ZVN2115B	N		150	16.000	0.42	39	SD1113HD
ZVN2117A	N		170	10.000	0.17	92	SD1113BD
ZVN2117B	N		170	10.000	0.46	39	SD1113HD
ZVN2120A	N		200	10.000	0.17	92	SD1113BD
ZVN2120B	N		200	10.000	0.46	39	SD1113HD
ZVN2202B	N		20	0.500	4.80	39	SD3301HD
ZVN2204B	N		40	0.500	4.80	39	SD3301HD
ZVN2206B	N		60	0.500	4.80	39	SD3301HD
ZVN2208B	N		80	0.800	3.45	39	SD3300HD
ZVN2210B	N		100	0.800	3.45	39	SD3300HD
ZVN2530A	N		300	35.000	0.09	92	SD1101BD
ZVN2530B	N		300	35.000	0.24	39	SD1101HD
ZVN2535A	N		350	35.000	0.09	92	SD1101BD
ZVN2535B	N		350	35.000	0.24	39	SD1101HD
ZVN3302A	N		20	5.000	0.27	92	VN0104N3
ZVN3302B	N		20	5.000	0.75	39	SD1117HD
ZVN3304A	N		40	5.000	0.27	92	VN0104N3
ZVN3304B	N		40	5.000	0.75	39	SD1117HD
ZVN3306A	N		60	5.000	0.27	92	VN0106N3
ZVN3306B	N		60	5.000	0.75	39	SD1117HD
ZVN3310A	N		100	10.000	0.20	92	SD1107BD
ZVN3310B	N		100	10.000	0.50	39	SD1107HD
ZVN3315A	N		150	40.000	0.10	92	SD1113BD
ZVN3315B	N		150	40.000	0.25	39	SD1113HD
ZVP0102A	P		-20	5.000	-.28	92	SD2107BD
ZVP0102B	P		-20	5.000	-.76	39	SD2107HD
ZVP0104A	P		-40	8.000	-.27	92	VP0104N3
ZVP0104B	P		-40	8.000	-.62	39	SD2107HD
ZVP0104D	P		-40	8.000	0.00	CHIP	VP0104ND
ZVP0106A	P		-60	8.000	-.23	92	VP0106N3
ZVP0106B	P		-60	8.000	-.60	39	SD2107HD
ZVP0106D	P		-60	8.000	0.00	CHIP	VP0106ND
ZVP0108A	P		-80	8.000	-.23	92	VP0109N3
ZVP0108B	P		-80	8.000	-.60	39	SD2107HD
ZVP0108D	P		-80	8.000	0.00	CHIP	VP0109ND
ZVP0109A	P		-90	8.000	-.27	92	VP0109N3
ZVP0109B	P		-90	8.000	-.62	39	SD2107HD
ZVP0110A	P		-100	16.000	-.20	92	SD2107BD
ZVP0110B	P		-100	16.000	-.44	39	SD2107HD
ZVP0110D	P		-100	16.000	0.00	CHIP	SD2107CHP
ZVP0204B	P		-40	4.000	-1.00	39	SD2107HD
ZVP0204D	P		-40	4.000	0.00	CHIP	SD2107CHP
ZVP0206B	P		-60	4.000	-1.00	39	SD2107HD
ZVP0206D	P		-60	4.000	0.00	CHIP	SD2107CHP
ZVP0208B	P		-80	4.000	-1.00	39	SD2107HD

Ferranti (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
ZVP0208D	P		-80	4.000	0.00	CHIP	SD2107CHP
ZVP0209B	P		-90	4.000	-1.00	39	SD2107HD
ZVP0210B	P		-100	8.000	-.64	39	SD2107HD
ZVP0210D	P		-100	8.000	0.00	CHIP	SD2107CHP
ZVP1110B	P		-100	4.000	-.97	39	SD2107HD
ZVP1110D	P		-100	4.000	0.00	CHIP	SD2107CHP
ZVP1404A	P		-40	600.000	-.03	92	SD2204BD
ZVP1406A	P		-60	600.000	-.03	92	SD2204BD
ZVP1408A	P		-80	600.000	-.03	92	SD2204BD
ZVP1409A	P		-90	600.000	-.03	92	SD2204BD
ZVP1410A	P		-100	1200.000	-.02	92	SD2204BD
ZVP1414A	P		-140	1200.000	-.02	92	SD2204BD
ZVP1416A	P		-160	2400.000	-.02	92	SD2204BD
ZVP1420A	P		-200	2400.000	-.02	92	SD2204BD
ZVP2104A	P		-40	5.000	-.28	92	SD2107BD
ZVP2104B	P		-40	5.000	-.76	39	SD2107HD
ZVP2106A	P		-60	5.000	-.28	92	SD2107BD
ZVP2106B	P		-60	5.000	-.76	39	SD2107HD
ZVP2110A	P		-100	8.000	-.23	92	SD2107BD
ZVP2110B	P		-100	8.000	-.60	39	SD2107HD
ZVP3302A	P		-20	14.000	-.16	92	VP0104N3
ZVP3304A	P		-40	14.000	-.16	92	VP0104N3
ZVP3306A	P		-60	14.000	-.16	92	VP0106N3

General Electric/Intersil

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
D80AK2	N		60	2.400	0.50	237	CF
IRFF110	N		100	0.600	3.50	205	SD3300HD
IRFF111	N		60	0.600	3.50	205	SD3301HD
IRFF112	N		100	0.800	3.00	205	SD3300HD
IRFF113	N		60	0.800	3.00	205	SD3301HD
IRFF123	N		60	0.400	5.00	205	SD3301HD
IVN5000AND	N		40	2.500	0.70	237	CF
IVN5000ANE	N		60	2.500	0.70	237	CF
IVN5000ANF	N		80	2.500	0.70	237	CF
IVN5000ANH	N		100	2.500	0.70	237	CF
IVN5000SND	N		40	2.500	0.90	52	SD1117DD
IVN5000SNE	N		60	2.500	0.90	52	SD1117DD
IVN5000TND	N		40	2.500	1.20	39	SD1117HD
IVN5000TNE	N		60	2.500	1.20	39	SD1117HD
IVN5000TNF	N		80	2.500	1.20	39	CF
IVN5000TNG	N		90	2.500	1.20	39	CF
IVN5000TNH	N		100	2.500	1.20	39	CF
IVN5001AND	N		40	2.500	0.70	237	CF
IVN5001ANE	N		60	2.500	0.70	237	CF
IVN5001ANF	N		80	2.500	0.70	237	CF
IVN5001ANH	N		100	2.500	0.70	237	CF
IVN5001SND	N		40	2.500	0.90	52	SD1117DD
IVN5001SNE	N		60	2.500	0.90	52	SD1117DD
IVN5001TND	N		40	2.500	1.20	39	SD1117HD
IVN5001TNE	N		60	2.500	1.20	39	SD1117HD
IVN5001TNF	N		80	2.500	1.20	39	SD1117HD
IVN5001TNG	N		90	2.500	1.20	39	SD1107HD
IVN5200TND	N		40	0.500	4.00	205	SD3301HD
IVN5200TNE	N		60	0.500	4.00	205	SD3301HD
IVN5200TNF	N		80	0.500	4.00	205	SD3300HD

General Electric/Intersil (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
IVN5201TND	N		40	0.500	4.00	205	SD3301HD
IVN5201TNE	N		60	0.500	4.00	205	SD3301HD
IVN5201TNF	N		80	0.500	4.00	205	SD3300HD
IVN6300ANE	N		60	7.500	0.25	237	SD1106AD
IVN6300ANF	N		80	7.500	0.25	237	SD1106AD
IVN6300SNE	N		60	7.500	0.25	52	SD1107DD
IVN6300SNF	N		80	7.500	0.25	52	SD1107DD
IVN6300SNH	N		100	7.500	0.25	52	SD1107DD
IVN6300SNM	N		200	25.000	0.12	52	SD1113DD
IVN6300SNP	N		250	25.000	0.12	52	SD1102DD
IVN6300SNS	N		400	75.000	0.10	52	SD1101DD
IVN6300SNT	N		450	75.000	0.10	52	SD1100DD
IVN6660	N	Z	60	3.000	2.40	39	SD1117HD
IVN6661	N	Z	90	4.000	2.40	39	SD1107HD
VN10KMA	N		60	5.000	0.75	237	SD1106AD

Hitachi

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2SK196H	N	Z	160	15.000	0.50	205	SD1113HD
2SK441	N		500	50.000	0.30	205	CF
2N6782	N		100	0.600	3.50	205	2N6782

International Rectifier

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
IRFC110	N		100	0.600	0.00	CHIP	SD3300CHP
IRFC113	N		60	0.800	0.00	CHIP	SD3301CHP
IRFC123	N		60	0.400	0.00	CHIP	SD3301CHP
IRFC1Z0	N		100	2.400	0.00	CHIP	CF
IRFC1Z3	N		60	3.200	0.00	CHIP	SD1117CHP
IRFF110	N		100	0.600	3.50	205	SD3300HD
IRFF111	N		60	0.600	3.50	205	SD3301HD
IRFF112	N		100	0.800	3.00	205	SD3300HD
IRFF113	N		60	0.800	3.00	205	SD3301HD
IRFF123	N		60	0.400	5.00	205	SD3301HD
IRFG1Z0	N	QUAD	100	2.600	0.45	CDIP	CF
IRFG1Z3	N	QUAD	60	3.400	0.38	CDIP	CF

ITT Semiconductor

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
BS107	N		200	28.000	0.08	92LF	SD1122BD
BS170	N		60	5.000	0.19	92LF	SD1124BD
BS250	P		-45	14.000	-.13	92LF	VP0106N3

VERTICAL and LATERAL D-MOS FET SUBSTITUTION GUIDE

Motorola

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6660	N		60	3.000	2.00	205	SD1117HD
2N6661	N		90	4.000	2.00	205	SD1107HD
BS107	N		200	28.000	0.25	226	SD1122BD
BS107A	N		200	6.000	0.25	226	CF
BS170	N		60	5.000	0.50	226	SD1124BD
MFE910	N		60	5.000	0.50	205	SD1117HD
MFE9200	N		200	6.400	0.40	206	SD1112DD
MFE930	N		35	1.400	2.00	205	SD3301HD
MFE960	N		60	1.700	2.00	205	SD3301HD
MFE990	N		90	2.000	2.00	205	SD3300HD
MPF6660	N		60	3.000	0.30	226	SD1117BD
MPF6661	N		90	4.000	0.25	226	SD1107BD
MPF910	N		60	5.000	0.20	226	SD1107BD
MPF9200	N		200	6.400	0.40	226	SD1112BD
MPF930	N		35	1.400	2.00	226	SD3301BD
MPF960	N		60	1.700	2.00	226	SD3301BD
MPF990	N		90	2.000	2.00	226	SD3300BD

RCA

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6782	N		100	0.600	3.50	205	2N6782
IRFF110	N		100	0.600	3.50	205	SD3300HD
IRFF111	N		60	0.600	3.50	205	SD3301HD
IRFF112	N		100	0.800	3.00	205	SD3300HD
IRFF113	N		60	0.800	3.00	205	SD3301HD
IRFF123	N		60	0.400	5.00	205	SD3301HD
RFL1N08L	N		80	1.200	1.00	205	SD3300HD
RFL1N10L	N		100	1.200	1.00	205	SD3300HD
RFL2N05	N		50	0.750	2.00	205	SD3301HD
RFL2N06	N		60	0.750	2.00	205	SD3301HD

Semi Processes, Inc.

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD1100CHP	N		450	35.000	0.00	CHIP	SD1100CHP
SD1100DD	N		450	35.000	0.08	18	SD1100DD
SD1100HD	N		450	35.000	0.08	39	SD1100HD
SD1101BD	N		400	25.000	0.08	92	SD1101BD
SD1101CHP	N		400	25.000	0.00	CHIP	SD1101CHP
SD1101DD	N		400	25.000	0.08	18	SD1101DD
SD1101HD	N		400	25.000	0.14	39	SD1101HD
SD1102BD	N		250	10.000	0.23	92	SD1102BD
SD1102CHP	N		250	10.000	0.00	CHIP	SD1102CHP
SD1102DD	N		250	10.000	0.31	18	SD1102DD
SD1102HD	N		250	10.000	0.57	39	SD1102HD
SD1104BD	N		100	3.000	0.42	92	SD1104BD
SD1104CHP	N		100	3.000	0.00	CHIP	SD1104CHP
SD1104DD	N		100	3.000	0.56	18	SD1104DD
SD1104HD	N		100	3.000	1.05	39	SD1104HD
SD1105BD	N		100	4.000	0.36	92	SD1105BD
SD1105CHP	N		100	4.000	0.00	CHIP	SD1105CHP
SD1105DD	N		100	4.000	0.49	18	SD1105DD
SD1105HD	N		100	4.000	0.91	39	SD1105HD
SD1106AD	N		60	5.000	0.50	237	SD1106AD

Semi Processes, Inc. (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD1106CHP	N		60	5.000	0.00	CHIP	SD1106CHP
SD1106DD	N		60	5.000	0.50	18	SD1106DD
SD1107BD	N		100	4.000	0.36	92	SD1107BD
SD1107CHP	N		100	4.000	0.00	CHIP	SD1107CHP
SD1107DD	N		100	4.000	0.49	18	SD1107DD
SD1107HD	N		100	4.000	0.91	39	SD1107HD
SD1107N	N	QUAD	100	4.000	0.51	PDIP	SD1107N
SD1112BD	N		200	7.000	0.27	92	SD1112BD
SD1112CHP	N		200	7.000	0.00	CHIP	SD1112CHP
SD1112DD	N		200	7.000	0.37	18	SD1112DD
SD1112HD	N		200	7.000	0.69	39	SD1112HD
SD1113BD	N		200	10.000	0.23	92	SD1113BD
SD1113CHP	N		200	10.000	0.00	CHIP	SD1113CHP
SD1113DD	N		200	10.000	0.31	18	SD1113DD
SD1113HD	N		200	10.000	0.57	39	SD1113HD
SD1114BD	N		80	3.000	0.42	92	SD1114BD
SD1114CHP	N		80	3.000	0.00	CHIP	SD1114CHP
SD1114DD	N		80	3.000	0.56	18	SD1114DD
SD1114HD	N		80	3.000	1.05	39	SD1114HD
SD1115BD	N		80	4.000	0.42	92	SD1115BD
SD1115CHP	N		80	4.000	0.00	CHIP	SD1115CHP
SD1115DD	N		80	4.000	0.49	18	SD1115DD
SD1115HD	N		80	4.000	0.91	39	SD1115HD
SD1117BD	N		60	2.500	0.46	92	SD1117BD
SD1117CHP	N		60	2.500	0.00	CHIP	SD1117CHP
SD1117DD	N		60	2.500	0.62	18	SD1117DD
SD1117HD	N		60	2.500	1.15	39	SD1117HD
SD1117N	N	QUAD	60	2.500	0.46	PDIP	SD1117N
SD1122BD	N		200	10.000	0.12	92LF	SD1122BD
SD1122CHP	N		200	10.000	0.00	CHIP	SD1122CHP
SD1124BD	N		60	5.000	0.20	92LF	SD1124BD
SD1124CHP	N		60	5.000	0.00	CHIP	SD1124CHP
SD1200CHP	N		450	700.000	0.00	CHIP	SD1200CHP
SD1200DD	N		450	700.000	0.02	18	SD1200DD
SD1201CHP	N		400	500.000	0.00	CHIP	SD1201CHP
SD1201DD	N		400	500.000	0.02	18	SD1201DD
SD1202BD	N		200	250.000	0.04	92	SD1202BD
SD1202CHP	N		200	250.000	0.00	CHIP	SD1202CHP
SD200DC/R	N		25	50.000	0.05	52+	SD200DC/R
SD201DC/R	N	Z	25	50.000	0.05	52+	SD201DC/R
SD202DC/R	N		20	35.000	0.05	52+	SD202DC/R
SD203DC/R	N	Z	20	35.000	0.05	52+	SD203DC/R
SD210DE/R	N		30	70.000	0.05	72	SD210DE/R
SD211DE/R	N	Z	30	70.000	0.05	72	SD211DE/R
SD212DE/R	N		10	70.000	0.05	72	SD212DE/R
SD213DE/R	N	Z	10	70.000	0.05	72	SD213DE/R
SD214DE/R	N		20	70.000	0.05	72	SD214DE/R
SD214EE	N		20	70.000	0.05	72	SD214DE
SD215DE/R	N	Z	20	70.000	0.05	72	SD215DE/R
SD303DC/R	N	Z DG	20	80.000	0.05	52+	SD303DC/R
SD304DE/R	N	Z DG	25	130.000	0.05	72	SD304DE/R
SD306DE/R	N	Z DG	20	100.000	0.05	72	SD306DE/R

SGS

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SGSP151	N		100	0.600	5.00	205	SD3300HD
SGSP152	N		80	0.600	5.00	205	SD3301HD

Signetics

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
DMP4025DB	N		25	6.000	0.80	39	SD205HD
DMS4025DE	N		25	6.000	0.20	72	SD217DE
SD200DC	N		25	50.000	0.05	52+	SD200DC
SD201DC	N	Z	25	50.000	0.05	52+	SD201DC
SD202DC	N		20	35.000	0.05	52+	SD202DC
SD203DC	N	Z	20	35.000	0.05	52+	SD203DC
SD210DE	N		30	70.000	0.05	72	SD210DE
SD210EE	N		30	70.000	0.05	72	SD210DE
SD211DE	N	Z	30	70.000	0.05	72	SD211DE
SD211EE	N	Z	30	70.000	0.05	72	SD211DE
SD212DE	N		10	70.000	0.05	72	SD212DE
SD212EE	N		10	70.000	0.05	72	SD212DE
SD213DE	N	Z	10	70.000	0.05	72	SD213DE
SD213EE	N	Z	10	70.000	0.05	72	SD213DE
SD214DE	N		20	70.000	0.05	72	SD214DE
SD215DE	N	Z	20	70.000	0.05	72	SD215DE
SD215EE	N	Z	20	70.000	0.05	72	SD215DE
SD217DE	N	Z	25	6.000	0.30	72	SD217DE
SD217EE	N	Z	25	6.000	0.30	72	SD217DE
SD220H	N		60	9.000	0.50	39	SD220HD
SD222DC	N		60	9.000	0.50	72	CF
SD300DC	N	Z DG	25	130.000	0.05	52+	SD304DE
SD300EC	N	Z DG	25	130.000	0.05	52+	SD304DE
SD303DC	N	Z DG	20	80.000	0.05	52+	SD303DC
SD303EC	N	Z DG	20	80.000	0.05	52+	SD303DC
SD304DE	N	Z DG	25	130.000	0.05	72	SD304DE
SD304EE	N	Z DG	25	130.000	0.05	72	SD304DE
SD306DE	N	Z DG	20	100.000	0.05	72	SD306DE
SD306EE	N	Z DG	20	100.000	0.05	72	SD306DE
SD5000I	N	Z QUAD	20	70.000	0.05	CDIP	SD5000J
SD5000N	N	Z QUAD	20	70.000	0.05	PDIP	SD5000N
SD5001I	N	Z QUAD	10	70.000	0.05	CDIP	SD5001J
SD5001N	N	Z QUAD	10	70.000	0.05	PDIP	SD5001N
SD5002I	N	Z QUAD	15	70.000	0.05	CDIP	SD5002J
SD5002N	N	Z QUAD	15	70.000	0.05	PDIP	SD5002N
SD5100N	N	Z QUAD	30	70.000	0.05	PDIP	SD5100N
SD5101N	N	Z QUAD	15	70.000	0.05	PDIP	SD5101N
SD5200I	N	Z QUAD	30	80.000	0.05	CDIP	CF
SD5200N	N	Z QUAD	30	80.000	0.05	PDIP	SD5200N

Siliconix

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6659	N		35	1.800	1.40	205	CF
2N6660	N		60	3.000	2.00	205	SD1117HD
2N6661	N		90	4.000	2.00	205	SD1107HD
2N6781	N		60	0.600	3.50	205	2N6781
2N6782	N		100	0.600	3.50	205	2N6782
2N7000	N		60	5.000	0.20	92	2N7000
2N7010	N		60	0.350	1.30	237	CF
2N7011	N		40	0.350	1.30	237	CF
2N7104	N	(210)	30	70.000	0.05	72	2N7104
2N7105	N	Z (211)	30	70.000	0.05	72	2N7105
2N7106	N	(212)	10	70.000	0.05	72	2N7106
2N7107	N	Z (213)	10	70.000	0.05	72	2N7107
2N7108	N	(214)	10	70.000	0.05	72	2N7108
2N7109	N	Z (215)	10	70.000	0.05	72	2N7109
2N7116	N	Z QUAD	20	70.000	0.05	CDIP	2N7116

Siliconix (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N7117	N	Z QUAD	10	70.000	0.05	CDIP	2N7117
2N7118	N	Z QUAD	15	70.000	0.05	CDIP	2N7118
BS107	N		200	28.000	0.08	92LF	SD1122BD
BS170	N		60	5.000	0.19	92LF	SD1124BD
BS250	P		-45	14.000	-.13	92LF	VP0106N3
BSR64	N		60	7.500	0.25	237	SD1106AD
BSR65	N		60	5.000	0.30	237	SD1106AD
BSR66	N		60	3.000	0.47	237	SD1106AD
BSR67	N		80	4.000	0.40	237	SD1106AD
IRFF110	N		100	0.600	3.50	205	SD3300HD
IRFF111	N		60	0.600	3.50	205	SD3301HD
IRFF112	N		100	0.800	3.00	205	SD3300HD
IRFF113	N		60	0.800	3.00	205	SD3301HD
IRFF123	N		60	0.400	5.00	205	SD3301HD
SD2100	N	DEPL	25	200.000	0.05	72	SD2100DE
SD210DE	N		30	70.000	0.05	72	SD210DE/R
SD2110	N	DUAL	25	60.000	0.05	78	SD411HD
SD211DE	N	Z	30	70.000	0.05	72	SD211DE/R
SD2120	N	DUAL	25	60.000	0.05	78	SD411HD
SD212DE	N		10	70.000	0.05	72	SD212DE/R
SD213DE	N	Z	10	70.000	0.05	72	SD213DE/R
SD214DE	N		20	70.000	0.05	72	SD214DE/R
SD215DE	N	Z	20	70.000	0.05	72	SD215DE/R
SD5000N	N	Z QUAD	20	70.000	0.05	PDIP	SD5000N
SD5001N	N	Z QUAD	10	70.000	0.05	PDIP	SD5001N
SD5002N	N	Z QUAD	15	70.000	0.05	PDIP	SD5002N
SD5200N	N	Z QUAD	30	80.000	0.05	PDIP	SD5200N
SD5400CY	N	Z QUAD	20	70.000	0.05	SO14	SD5400CY
SD5401CY	N	Z QUAD	10	70.000	0.05	SO14	SD5401CY
SD5402CY	N	Z QUAD	15	70.000	0.05	SO14	SD5402CY
SI2200	N		15	16.000	0.00	72	SD217DE
SI2400	N	Z	15	12.000	0.05	72	SD217DE
SN0120NB	N	OCTAL	200	300.000	0.05	CDIP	AN0120NA
SN0130NB	N	OCTAL	300	300.000	0.05	CDIP	AN0130NA
SN0140NB	N	OCTAL	400	350.000	0.05	CDIP	AN0140NA
SST211	N	Z SOT	30	75.000	0.05	143	CF
SST213	N	Z SOT	10	75.000	0.05	143	CF
SST215	N	Z SOT	20	75.000	0.05	143	CF
VN0300B	N		30	1.200	1.86	205	SD3301HD
VN0300L	N		30	1.200	0.63	92	SD3301BD
VN0300M	N		30	1.200	0.75	237	SD3301AD
VN0606M	N		60	3.000	0.47	237	SD1106AD
VN0610L	N	Z	60	5.000	0.19	92	SD1117BD
VN0610LL	N		60	5.000	0.19	92	VN0610LL
VN0808M	N		80	4.000	0.40	237	CF
VN10KE	N	Z	60	5.000	0.17	52	SD1107DD
VN10KM	N	Z	60	5.000	0.30	237	SD1106AD
VN10LE	N		60	5.000	0.17	52	SD1106DD
VN10LM	N		60	5.000	0.30	237	VN10LM
VN1206B	N		120	6.000	0.63	205	CF
VN1206L	N		120	6.000	0.16	92	CF
VN1206M	N		120	6.000	0.25	237	CF
VN1210L	N		120	10.000	0.12	92	VN2410L
VN1210M	N		120	10.000	0.19	237	CF
VN1706L	N		170	6.000	0.16	92	CF
VN1710L	N		170	10.000	0.12	92	VN2410L
VN1710M	N		170	10.000	0.19	237	CF
VN1720M	N		170	20.000	0.14	237	CF
VN2020L	N		200	24.000	0.08	92	CF
VN2222KM	N	Z	60	7.500	0.25	237	SD1106AD

Siliconix (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
VN2222L	N	Z	60	7.500	0.15	92	SD1117BD
VN2222LL	N		60	7.500	0.15	92	VN2222LL
VN2222LM	N		60	7.500	0.25	237	VN2222LM
VN2406B	N		240	6.000	0.63	205	CF
VN2406L	N		240	6.000	0.16	92	CF
VN2406M	N		240	6.000	0.25	237	CF
VN2410L	N		240	10.000	0.12	92	VN2410L
VN2410M	N		240	10.000	0.19	237	CF
VN2420L	N		240	24.000	0.08	92	CF
VN35AB	N		35	2.500	1.29	205	SD1117HD
VN67AB	N		60	3.500	1.09	205	SD1117HD
VN90AB	N		90	5.000	0.91	205	SD1107HD
VN99AB	N		90	4.500	0.96	205	SD1107HD
VNC010B	N		60	0.500	4.00	205	SD3301HD
VNC011B	N		60	0.500	4.00	205	SD3301HD
VND010B	N		80	0.500	4.00	205	SD3300HD
VND011B	N		80	0.500	4.00	205	SD3300HD
VNE010B	N		100	0.500	4.00	205	SD3300HD
VNE011B	N		100	0.500	4.00	205	SD3300HD
VP0808B	P		-80	5.000	-.88	205	SD2107HD
VP0808L	P		-80	5.000	-.21	92	VP0808L
VP0808M	P		-80	5.000	-.33	237	VP0808M
VP1008B	P		-100	5.000	-.88	205	SD2107HD
VP1008L	P		-100	5.000	-.21	92	VP1008L
VP1008M	P		-100	5.000	-.33	237	VP1008M
VQ1000J	N	QUAD	60	5.500	0.22	PDIP	VQ1000J
VQ1004J	N	QUAD	60	3.500	0.46	PDIP	SD1117N
VQ1006J	N	QUAD	60	4.500	0.40	PDIP	SD1107N
VQ2004J	P	QUAD	-60	5.000	-.41	PDIP	CF
VQ2006J	P	QUAD	-90	5.000	-.41	PDIP	CF

Supertex

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6659	N		35	1.800	1.40	205	CF
2N6660	N		60	3.000	2.00	205	SD1117HD
2N6661	N		90	4.000	2.00	205	SD1107HD
2N7000	N		50	5.000	0.20	92	2N7000
2N7007	N		240	45.000	0.15	92	VN2410L
2N7008	N		60	7.500	0.30	92	CF
AN0116NA	N	OCTAL	160	350.000	0.03	PDIP	AN0120NA
AN0116NB	N	OCTAL	160	350.000	0.03	CDIP	AN0120NA
AN0120NA	N	OCTAL	200	300.000	0.03	PDIP	AN0120NA
AN0120NB	N	OCTAL	200	300.000	0.04	CDIP	AN0120NA
AN0130NA	N	OCTAL	300	300.000	0.03	PDIP	AN0130NA
AN0130NB	N	OCTAL	300	300.000	0.04	CDIP	AN0130NA
AN0132NA	N	OCTAL	320	350.000	0.03	PDIP	AN0140NA
AN0132NB	N	OCTAL	320	350.000	0.03	CDIP	AN0140NA
AN0140NA	N	OCTAL	400	350.000	0.03	PDIP	AN0140NA
AN0140NB	N	OCTAL	400	350.000	0.04	CDIP	AN0140NA
AP0116NA	P	OCTAL	-160	700.000	-.01	PDIP	AP0120NA
AP0116NB	P	OCTAL	-160	700.000	-.01	CDIP	AP0120NA
AP0120NA	P	OCTAL	-200	600.000	-.01	PDIP	AP0120NA
AP0120NB	P	OCTAL	-200	600.000	-.01	CDIP	AP0120NA
AP0130NA	P	OCTAL	-300	600.000	-.01	PDIP	AP0130NA
AP0130NB	P	OCTAL	-300	600.000	-.01	CDIP	AP0130NA
AP0132NA	P	OCTAL	-320	700.000	-.01	PDIP	AP0140NA
AP0132NB	P	OCTAL	-320	700.000	-.01	CDIP	AP0140NA
TN0106N2	N		60	3.000	0.80	39	CF

Supertex (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
TN0106N3	N		60	3.000	0.35	92	TN0106N3
TN0106ND	N		60	3.000	0.00	CHIP	TN0106ND
TN0110N2	N		100	3.000	0.80	39	CF
TN0110N3	N		100	3.000	0.50	92	TN0110N3
TN0110ND	N		100	3.000	0.00	CHIP	TN0110ND
TN0520N2	N		200	10.000	1.00	39	CF
TN0520N3	N		200	10.000	0.30	92	VN2410L
TN0520ND	N		200	10.000	0.00	CHIP	CF
TN0524N2	N		240	10.000	0.70	39	CF
TN0524N3	N		240	10.000	0.30	92	VN2410L
TN0524ND	N		240	10.000	0.00	CHIP	CF
TN0620N2	N		200	6.000	0.70	39	CF
TN0620N3	N		200	6.000	0.40	92	CF
TN0620ND	N		200	6.000	0.00	CHIP	CF
TN0624N2	N		240	6.000	0.70	39	CF
TN0624N3	N		240	6.000	0.40	92	CF
TN0624ND	N		240	6.000	0.00	CHIP	CF
VN0104N2	N		40	3.000	0.80	39	SD1117HD
VN0104N3	N		40	3.000	0.50	92	VN0104N3
VN0104ND	N		40	3.000	0.00	CHIP	VN0104ND
VN0106N2	N		60	3.000	0.80	39	SD1117HD
VN0106N3	N		60	3.000	0.50	92	VN0106N3
VN0106ND	N		60	3.000	0.00	CHIP	VN0106ND
VN0109N2	N		90	3.000	0.80	39	CF
VN0109N3	N		90	3.000	0.50	92	VN0109N3
VN0109ND	N		90	3.000	0.00	CHIP	VN0109ND
VN0110N2	N		100	8.000	0.50	39	SD1107HD
VN0110N3	N		100	8.000	0.30	92	SD1107BD
VN0114N2	N		140	8.000	0.50	39	SD1112HD
VN0114N3	N		140	8.000	0.30	92	SD1112BD
VN0116N2	N		160	10.000	0.35	39	SD1113HD
VN0116N3	N		160	10.000	0.25	92	SD1113BD
VN0116ND	N		160	10.000	0.00	CHIP	SD1113CHP
VN0120N2	N		200	10.000	0.35	39	SD1113HD
VN0120N3	N		200	10.000	0.25	92	SD1113BD
VN0120ND	N		200	10.000	0.00	CHIP	SD1113CHP
VN0204N2	N		40	2.000	1.50	39	SD1117HD
VN0204ND	N		40	2.000	0.00	CHIP	SD1117CHP
VN0206N2	N		60	2.000	1.50	39	SD1117HD
VN0206N3	N		60	2.000	0.80	92	SD1117BD
VN0206ND	N		60	2.000	0.00	CHIP	SD1117CHP
VN0216N2	N		160	6.000	0.70	39	SD1112HD
VN0216N3	N		160	6.000	0.40	92	SD1112BD
VN0216ND	N		160	6.000	0.00	CHIP	SD1112CHP
VN0220N2	N		200	6.000	0.70	39	SD1112HD
VN0220N3	N		200	6.000	0.40	92	SD1112BD
VN0220ND	N		200	6.000	0.00	CHIP	SD1112CHP
VN0300B	N		30	1.200	1.86	205	SD3301HD
VN0300L	N		30	1.200	0.63	92	SD3301BD
VN0530N2	N		300	50.000	0.25	39	SD1101HD
VN0530N3	N		300	50.000	0.10	92	SD1101BD
VN0530ND	N		300	50.000	0.00	CHIP	SD1101CHP
VN0535N2	N		350	35.000	0.25	39	SD1101HD
VN0535N3	N		350	35.000	0.10	92	SD1101BD
VN0535ND	N		350	35.000	0.00	CHIP	SD1101CHP
VN0540N2	N		400	35.000	0.25	39	SD1101HD
VN0540N3	N		400	35.000	0.10	92	SD1101BD
VN0540ND	N		400	35.000	0.00	CHIP	SD1101CHP
VN0545N2	N		450	60.000	0.10	39	CF
VN0545N3	N		450	60.000	0.10	92	SD1501BD
VN0545ND	N		450	60.000	0.00	CHIP	SD1501CHP

Supertex (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
VN0550N3	N		500	60.000	0.05	92	SD1501BD
VN0550ND	N		500	60.000	0.00	CHIP	SD1501CHP
VN0606M	N		60	3.000	0.47	237	SD1106AD
VN0610L	N		60	5.000	0.19	92	VN0610LL
VN0808M	N		80	4.000	0.40	237	CF
VN10KN3	N		60	5.000	0.30	92	VN10KN3
VN10KN9	N		60	5.000	0.30	52	SD1106DD
VN1106N2	N		60	0.700	2.50	205	SD3301HD
VN1106ND	N		60	0.700	0.00	CHIP	SD3301CHP
VN1110N2	N		100	0.700	2.50	205	SD3300HD
VN1110ND	N		100	0.700	0.00	CHIP	SD3300CHP
VN1210B	N		120	10.000	0.40	205	CF
VN1210L	N		120	10.000	0.12	92	VN2410L
VN1304N2	N		40	8.000	0.40	39	SD1117HD
VN1304N3	N		40	8.000	0.25	92	SD1117BD
VN1304ND	N		40	8.000	0.00	CHIP	SD1117CHP
VN1306N2	N		60	8.000	0.40	39	SD1117HD
VN1306N3	N		60	8.000	0.25	92	SD1117BD
VN1306ND	N		60	8.000	0.00	CHIP	SD1117CHP
VN1310N2	N		100	8.000	0.40	39	SD1107HD
VN1310N3	N		100	8.000	0.25	92	SD1107BD
VN1310ND	N		100	8.000	0.00	CHIP	SD1107CHP
VN1316N2	N		160	40.000	0.15	39	SD1113HD
VN1316N3	N		160	40.000	0.10	92	SD1113BD
VN1316ND	N		160	40.000	0.00	CHIP	SD1113CHP
VN1320N2	N		200	40.000	0.15	39	SD1113HD
VN1320N3	N		200	40.000	0.10	92	SD1113BD
VN1320ND	N		200	40.000	0.00	CHIP	SD1113CHP
VN1710B	N		170	10.000	0.60	205	CF
VN2010L	N		200	10.000	0.12	92	VN2410L
VN2106ND	N		60	3.000	0.00	CHIP	SD1117CHP
VN2110ND	N		100	3.000	0.00	CHIP	TN0110ND
VN2222L	N		60	7.500	0.15	92	VN2222LL
VN2406B	N		240	6.000	0.40	39	CF
VN2406L	N		240	6.000	0.25	92	CF
VN2410L	N		240	6.000	0.12	92	VN2410L
VP0104N2	P		-40	8.000	-.50	39	SD2107HD
VP0104N3	P		-40	8.000	-.40	92	VP0104N3
VP0104ND	P		-40	8.000	0.00	CHIP	VP0104ND
VP0106N2	P		-60	8.000	-.50	39	SD2107HD
VP0106N3	P		-60	8.000	-.40	92	VP0106N3
VP0106ND	P		-60	8.000	0.00	CHIP	VP0106ND
VP0109N2	P		-90	8.000	-.50	39	SD2107HD
VP0109N3	P		-90	8.000	-.40	92	VP0109N3
VP0109ND	P		-90	8.000	0.00	CHIP	VP0109ND
VP0110N2	P		-100	16.000	0.00	39	SD2107HD
VP0110N3	P		-100	16.000	0.00	92	SD2107BD
VP0110ND	P		-100	16.000	0.00	CHIP	SD2107CHP
VP0204N2	P		-40	4.000	-.80	39	SD2107HD
VP0204ND	P		-40	4.000	0.00	CHIP	SD2107CHP
VP0206N2	P		-60	4.000	-.80	39	SD2107HD
VP0206N3	P		-60	4.000	-.40	92	SD2107BD
VP0206ND	P		-60	4.000	0.00	CHIP	SD2107CHP
VP0210N2	P		-100	4.000	-.80	39	SD2107HD
VP0210N3	P		-100	4.000	-.40	92	SD2107BD
VP0210ND	P		-100	4.000	0.00	CHIP	SD2107CHP
VP0808B	P		-80	5.000	-.88	39	SD2107HD
VP0808L	P		-80	5.000	-.21	92	SD2107BD
VP1008B	P		-100	5.000	-.88	39	SD2107HD

Supertex (continued)

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
VP1008L	P		-100	5.000	-.21	92	SD2107BD
VQ1000N6	N	QUAD	60	5.500	0.30	PDIP	VQ1000J
VQ1000N7	N	QUAD	60	5.500	0.30	CDIP	VQ1000J
VQ1004J	N	QUAD	60	3.500	0.46	PDIP	SD1117N

Telmos

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
SD210CHP	N		30	70.000	0.00	CHIP	SD210CHP
SD210DE	N		30	70.000	0.05	72	SD210DE
SD210DE/R	N		30	70.000	0.05	72	SD210DE/R
SD211CHP	N	Z	30	70.000	0.00	CHIP	SD211CHP
SD211DE	N	Z	30	70.000	0.05	72	SD211DE
SD211DE/R	N	Z	30	70.000	0.05	72	SD211DE/R
SD212CHP	N		10	70.000	0.00	CHIP	SD212CHP
SD212DE	N		10	70.000	0.05	72	SD212DE
SD212DE/R	N		10	70.000	0.05	72	SD212DE/R
SD213CHP	N	Z	10	70.000	0.00	CHIP	SD213CHP
SD213DE	N	Z	10	70.000	0.05	72	SD213DE
SD213DE/R	N	Z	10	70.000	0.05	72	SD213DE/R
SD214CHP	N		20	70.000	0.00	CHIP	SD214CHP
SD214DE	N		20	70.000	0.05	72	SD214DE
SD214DE/R	N		20	70.000	0.05	72	SD214DE/R
SD215CHP	N	Z	20	70.000	0.00	CHIP	SD215CHP
SD215DE	N	Z	20	70.000	0.05	72	SD215DE
SD215DE/R	N	Z	20	70.000	0.05	72	SD215DE/R
SD5000CHP	N	Z QUAD	20	70.000	0.00	CHIP	SD5000CHP
SD5000J	N	Z QUAD	20	70.000	0.05	CDIP	SD5000J
SD5000N	N	Z QUAD	20	70.000	0.05	PDIP	SD5000N
SD5001CHP	N	Z QUAD	10	70.000	0.00	CHIP	SD5001CHP
SD5001J	N	Z QUAD	10	70.000	0.05	CDIP	SD5001J
SD5001N	N	Z QUAD	10	70.000	0.05	PDIP	SD5001N
SD5002CHP	N	Z QUAD	15	70.000	0.00	CHIP	SD5002CHP
SD5002J	N	Z QUAD	15	70.000	0.05	CDIP	SD5002J
SD5002N	N	Z QUAD	15	70.000	0.05	PDIP	SD5002N
SD5100CHP	N	Z QUAD	30	70.000	0.00	CHIP	SD5100CHP
SD5100N	N	Z QUAD	30	70.000	0.05	PDIP	SD5100N
SD5101CHP	N	Z QUAD	15	70.000	0.00	CHIP	SD5101CHP
SD5101N	N	Z QUAD	15	70.000	0.05	PDIP	SD5101N
SD5200CHP	N	Z QUAD	30	80.000	0.00	CHIP	SD5200CHP
SD5200N	N	Z QUAD	30	80.000	0.05	PDIP	SD5200N
TMF123	N	DUAL	20	100.000	0.05	99	SD411HD

Texas Instruments

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
PV210	N		35	2.500	1.50	39	SD1117HD
PV211	N		60	3.500	1.50	39	SD1117HD
PV212	N		80	4.500	1.50	39	SD1117HD
TIS172	N		35	1.600	0.30	92	SD3301BD
TIS173	N		60	2.000	0.30	92	SD1117BD
TIS72	N		35	1.800	0.30	92	SD3301BD
TIS73	N		60	2.500	0.25	92	SD1117BD
TIS74	N		80	3.500	0.20	92	SD1107BD

Texet Semiconductors

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
TX101	N		60	6.000	0.80	92	SD1107BD
TX102	N		100	6.000	0.80	92	SD1107BD
TX103	N		150	12.000	0.40	92	SD1113BD
TX104	N		200	12.000	0.40	92	SD1113BD
TX105	N		350	40.000	0.25	92	SD1101BD
TX106	N		400	40.000	0.25	92	SD1101BD
TX107	N		450	70.000	0.20	92	SD1501BD
TX108	N		500	70.000	0.20	92	SD1501BD

Toshiba

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2SK422	N		60	2.800	0.50	92	SD1117BD
2SK423	N		100	4.500	0.30	92	SD1107BD

Unitrode

PART NO.	CHAN.	DESCR.	(V) BV_{DSS}	(ohms) $r_{DS(on)}$	(Amps) $I_{D(on)}$	(TO-XX) PACKAGE	TOPAZ PART NUMBER
2N6781	N		60	0.600	3.50	205	2N6781
2N6782	N		100	0.600	3.50	205	2N6782
UFNF110	N		100	0.600	3.50	205	SD3300HD
UFNF111	N		60	0.600	3.50	205	SD3301HD
UFNF112	N		100	0.800	3.00	205	SD3300HD
UFNF113	N		60	0.800	3.00	205	SD3301HD
UFNF123	N		60	0.400	5.00	205	SD3301HD

N-Channel, Depletion-Mode, Lateral D-MOS FETs are suitable to replace N-Channel J-Fets under the following conditions:

(1) A negative voltage is available to bias the Body (Substrate) of the D-MOS FET to the most negative point in the circuit.

(2) The application requires faster switching speeds or wider operating bandwidth. J-FETs are still a better choice for low frequency applications where low 1/f Noise Voltage and low Gate Leakage below the I_G Breakpoint are the most important specifications.

(3) The application is not low frequency and requires wider dynamic or higher I_G Breakpoint. Depletion-Mode Lateral D-MOS does not have an I_G Breakpoint by design and can operate in enhancement or depletion mode provided that rated breakdown voltages are not exceeded.

J-FET Industry Part No.	Depletion D-MOS Replacement
2N2606-09	—
2N3328-32	—
2N3382/84/86	—
2N3684-87	—
2N3819	—
2N3821-24	SD2100DE
2N3921-22	—
2N3954-58	—
2N3954A-55A	—
2N3970-72	SD2100DE
2N3993-94	—
2N4084-85	—
2N4091-93	SD2100DE
2N4091A-93A	SD2100DE
ITE4091-93	—
PN4091-93	—
2N4117-19	—
PN4117-19	—
2N4117A-19A	—
FN4117A-19A	—
PN4117A-19A	—
2N4220-24	SD2100DE
2N4220A-22A	SD2100DE
2N4302-04	—
PN4302-04	—
2N4338-41	—
PN4338-41	—
2N4342-43	—
PN4342-43	—
2N4391-93	SD2100DE
FN4391-93	SD2100DE
ITE4391-93	—
PN4391-93	—
SST4391-93	—
2N4416	SD2100DE
ITE4416	—
PN4416	—
2N4856-61	SD2100DE
2N4856A-61A	—
2N4867-69	—
2N4867A-69A	—
2N4978	—
2N5018-19	—
2N5045-47	—
2N5114-16	—
PN5114-16	—
PN5163	—
2N5196-99	—
2N5265-70	—
2N5397-98	SD2100DE
2N5432-34	—
PN5432-34	—
2N5452-54	—
2N5457-59	—
SST5457-59	—
2N6460-65	—
2N5484-86	—
2N5515-24	—
2N5545-47	—
DN5564-66	TZ5911HD

J-FET Industry Part No.	Depletion D-MOS Replacement
2N5564-66	TZ5911HD
2N5555	—
DN5567	TZ5911HD
2N5638-40	—
2N5653-54	—
2N5902-09	—
2N5911-12	TZ5911HD
IT5911-12	TZ5911HD
ITC5911-12	TZ5911HD
M5911-12	TZ5911HD
2N6483-85	—
2N6905-07	—
2N6908-11	—
CR022-430	—
CRR0240-4300	—
DPAD series	—
IT100-01	—
IT500-05	—
IT550	TZ5911HD
Jxxx series	—
M440-441	TZ5911HD
MPF series	—
PAD series	—
U200-202	—
U231-235	—
U257	TZ5911HD
U290-91	—
U304-306	SD2200DE
U308-310	SD2200DE
U311	SD2200DE
U320-322	—
U350	SD5501N
U401-06	—
U410-12	—
U420-26	—
U427-28	—
U430-31	TZ5911HD
U440-42	TZ5911HD
U443-44	TZ5911HD
U1897-99	—
VCR series	—

TOPAZ SEMICONDUCTOR

2N6781, 2N6782

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-205 AF (TO-39) Hermetic Package	2N6782	2N6781
Description	100V, 0.6 ohm	60V, 0.6 ohm

FEATURES

- Gate Stand-off Voltage, ±40V min.
- Continuous I_D of 1 Amp in small package
- Wide Variety of Packages

APPLICATIONS

- Motor Controls
- Line Drivers
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Drain-Source Voltage
- 2N6782 ..... 100V*
- 2N6781 ..... 60V*

Drain-Gate Voltage (R_{GS} = 1MΩ)
- 2N6782 ..... 100V*
- 2N6781 ..... 60V*

Gate-Source Voltage ..... ±40V

Continuous Drain Current

T_C = +100°C	T_C = +25°C
2.25A*	3.5A*

Peak Pulsed Drain Current 8.0A

*JEDEC Registered Values

Maximum Power Dissipation

T_C = +100°C	T_C = +25°C
6.0W*	15W*

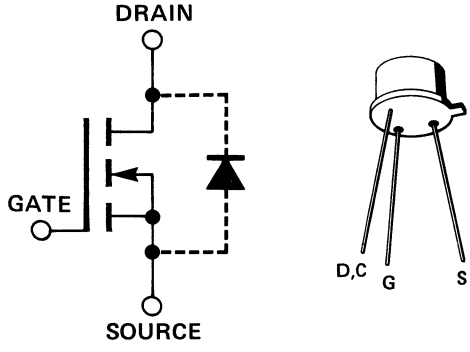
Linear Derating Factor

Junction to Ambient (mW/°C)	Junction to Case (mW/°C)
5.0*	120*

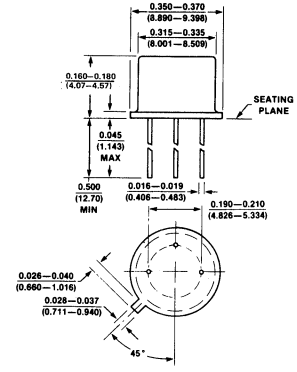
Operating Junction and Storage Temperature Range ..... -55 to +150°C*

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +300°C*

CONFIGURATION



PACKAGE DIMENSIONS TO-205 AF



All dimensions in inches and (millimeters)

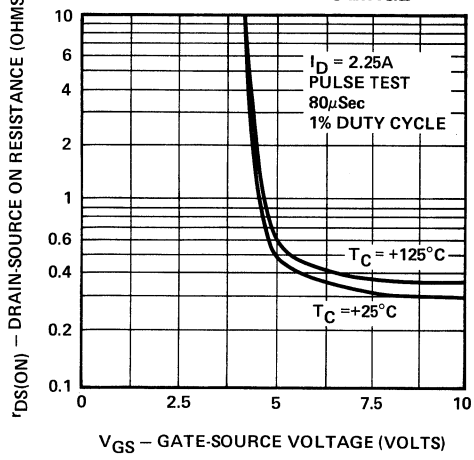
ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

#		CHARACTERISTIC	2N6782 MIN	2N6782 TYP	2N6782 MAX	2N6781 MIN	2N6781 TYP	2N6781 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	100*	125		60*	90		V	I_D = 250μA, V_{GS} = 0	
2		$V_{GS(th)}$ Gate-Source Threshold Voltage	2.0*		4.0*	2.0*		4.0*	V	V_{DS} = V_{GS}	
3			1.0*		4.0*	1.0*		4.0*		I_D = 250μA	T_C = +125°C
4		I_{GBS} Gate-Body Leakage Current			100*			100*	nA	V_{GS} = 20V, V_{DS} = 0	
5					200*			200*			T_C = +125°C
6					-100*			-100*		V_{GS} = -20V, V_{DS} = 0	
7		I_{DSS} Drain-Source OFF Leakage Current			0.25*				mA	V_{DS} = 80V, V_{GS} = 0	
8					1.0*					V_{DS} = 100V, V_{GS} = 0	T_C = +125°C
9								0.25*		V_{DS} = 48V, V_{GS} = 0	
10								1.0*		V_{DS} = 60V, V_{GS} = 0	T_C = +125°C
11		$I_{D(on)}$ ON Drain Current[1]	3.5*			3.5*			A	V_{DS} = 10V, V_{GS} = 10V	
12		$V_{DS(on)}$ Drain-Source[1] ON Voltage			2.1*			2.1*	V	V_{GS} = 10V, I_D = 3.5A	
13		$r_{DS(on)}$ Drain-Source[1] ON Resistance			0.6*			0.6*	ohms	V_{GS} = 10V	
14					1.08*			1.08*		I_D = 2.25A	T_C = +125°C
15	DYNAMIC	g_{fs} Common-Source[1] Forward Transcond.	1.0*		3.0*	1.0*		3.0*	S	V_{DS} = 10V, V_{GS} = 10V f = 1KHz	
16		C_{iss} Common-Source Input Capacitance	60*		200*	60*		200*	pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	
17		C_{rss} Common-Source Reverse Transfer Capacitance	10*		25*	10*		25*			
18		C_{oss} Common-Source Output Capacitance	40*		100*	40*		100*			
19		$t_{d(on)}$ Turn-ON Delay Time			15*			15*	nsec	V_{DD} = 34V R_L = 15 ohms R_G = 25 ohms $V_{G(on)}$ = 10V	
20		t_r Rise Time			25*			25*			
21		$t_{d(off)}$ Turn-OFF Delay Time			25*			25*			
22		t_f Fall Time			20*			20*			
23	DIODE	I_S Continuous Source Current[1]	3.5*			3.5*			A		
24		I_{SM} Peak Source Current[1]	8.0*			8.0*					
25		V_{SD} Source-Drain[1] Forward Voltage	0.75*		1.50*	0.75*		1.50*	V	V_{GS} = 0, I_S = 3.5A	
26		$R_{th\ J-C}$ Thermal Resistance Junction-to-Case			8.33*			8.33*	°C/W		
27		$R_{th\ J-A}$ Thermal Resistance Junction-to-Ambient			170			170	°C/W		

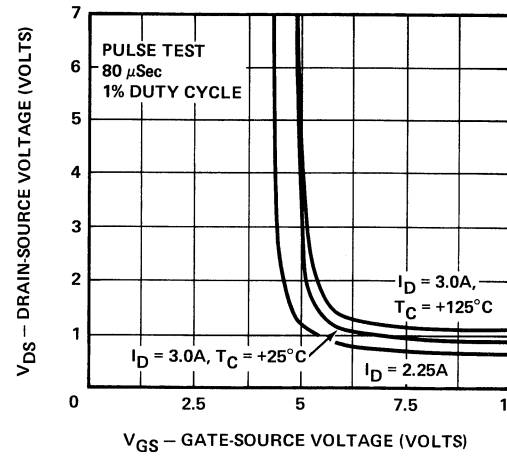
Note 1: Pulse Test 80μSec, 1% Duty Cycle *JEDEC Registered Values

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

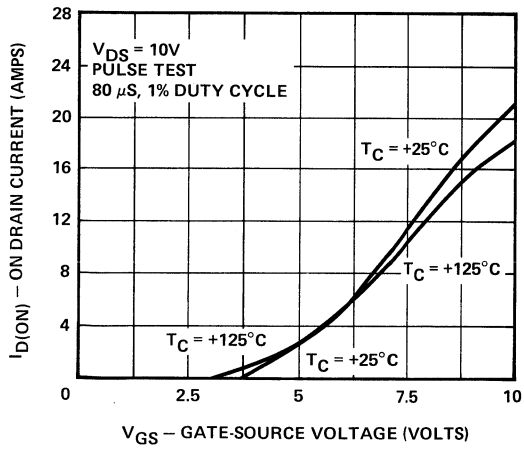
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



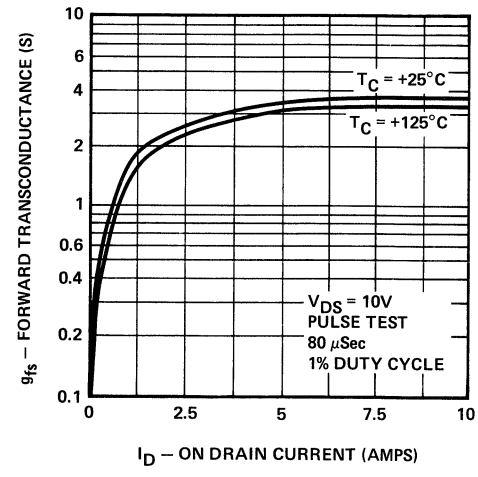
ON VOLTAGE CHARACTERISTICS



ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

2N7000

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- High Gate Oxide Breakdown, ±40V min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +60V

Drain-Gate Voltage (V_{GS}= 0) ..... +60V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

T_A = 25°C	T_C = 25°C
.21A	.32A

Peak Pulsed Drain Current 0.79A

Continuous Device Dissipation 400mW

Linear Derating Factor ..... 3.2mW/°C

Pulsed Device Dissipation 3.125W

Linear Derating Factor ..... 25mW/°C

Operating Junction Temperature Range ..... -55 to +150°C

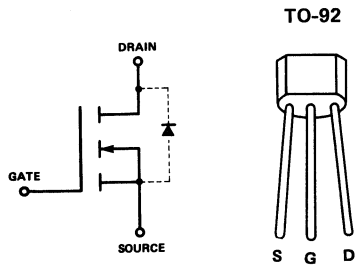
Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +300°C

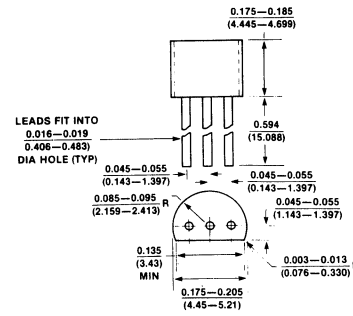
ORDERING INFORMATION

TO-92 Plastic Package	2N7000
Description	60V, 5 ohm

SCHEMATIC DIAGRAM/PACKAGE



PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		2N7000 MIN	2N7000 TYP	2N7000 MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60	100		V	I_D = 10μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8	1.9	3.0	V	I_D = 1.0mA, V_{DS} = V_{GS}
3		I_{GBS}	Gate-Body Leakage Current		±1.0	±10	nA	V_{GS} = ±15V, V_{DS} = 0
4		I_{DSS}	Drain-Source OFF		0.1	1.0	μA	V_{DS} = 48V, V_{GS} = 0
5			Leakage Current		.01	1.0	mA	T_A = +125°C
6		$I_{D(on)}$	ON Drain Current	75			mA	V_{DS} = 10V, V_{GS} = 4.5V (Note 1)
7		$V_{DS(on)}$	Drain-Source ON Voltage			0.4	V	V_{GS} = 4.5V, I_D = 75mA (Note 1)
8					1.5	2.5		V_{GS} = 10V, I_D = 0.5A (Note 1)
9		$r_{DS(on)}$	Drain-Source ON Resistance		3.0	5.0	ohms	V_{GS} = 10V, I_D = 0.5A (Note 1)
10					4.7	9.0		T_A = +125°C
11	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	100			mmhos	V_{DS} = 10V, I_D = 0.2A f = 1KHz (Note 1)
12		C_{iss}	Common-Source Input Capacitance			60	pF	V_{DS} = V_{GS} = 0 f = 1MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.3	5.0		
14		C_{OSS}	Common-Source Output Capacitance		10.5	25		
15		t_{on}	Turn-On Time		5.0	10	nSec	V_{DD} = 15V, $V_{G(on)}$ = 10V
16		t_{off}	Turn-Off Time		6.0	10		R_G = 25Ω, R_L = 25Ω

Note 1: Pulse Test 80μ Sec, 1% Duty Cycle

TOPAZ SEMICONDUCTOR

2N7104, 2N7105, 2N7106 2N7107, 2N7108, 2N7109

N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

TO-72 PACKAGE SHORTING RINGS ON LEADS		2N7104	2N7105+	2N7106	2N7107+	2N7108	2N7109+
Sorted chips in Waffle Pack		SD210CHP	SD21CHP	SD212CHP	SD213CHP	SD214CHP	SD215CHP
DESCRIPTION	BV_{DS} min.	30V	30V	10V	10V	20V	20V
	BV_{SD} min.	10V	10V	10V	10V	20V	20V
	$r_{DS(on)}$ max.	70 ohms	70 ohms	70 ohms	70 ohms	70 ohms	70 ohms

+ Gate Protective Diode

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low inter-electrode Capacitances

APPLICATIONS

- +30V Switch Drivers—2N7104, 2N7105
- ±10V Analog Switches —2N7108, 2N7109
- ±5V Analog Switches —2N7106, 2N7107

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	2N 7104	2N 7105	2N 7106	2N 7107	2N 7108	2N 7109	UNIT
Breakdown Voltages							
V_{DS}	+30	+30	+10	+10	+20	+20	V
V_{SD}	+10	+10	+10	+10	+20	+20	V
V_{DB}	+30	+30	+15	+15	+25	+25	V
V_{SB}	+15	+15	+15	+15	+25	+25	V
V_{GS}	±40*	−15	±40*	−15	±40*	−25	V
		+25		+25		+30	V
V_{GB}	±40	−0.3	±40	−0.3	±40	−0.3	V
		+25		+25		+30	V
V_{GD}	±40	−30	±40	−15	±40	−25	V
		+25		+25		+30	V
V_{DG}	+40*	+25*	+40*	+25*	+40*	+30*	V

I_D Continuous Drain Current 50mA*

P_T Power Dissipation (at or below T_c = +25°C) 1.2W

Linear Derating Factor ..... 12mW/°C

P_D Power Dissipation (at or below T_A = +25°C) 300mW*

Linear Derating Factor ..... 2.4 mW/°C*

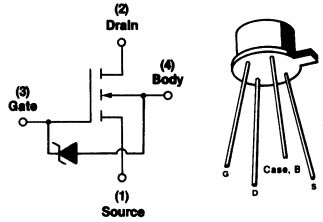
T_j Operating Junction Temperature Range ..... −55 to +150°C*

T_s Storage Temperature Range ..... −65 to +200°C

T_l Lead Temperature (1/16" from mounting surface for 10 sec) ..... +300°C

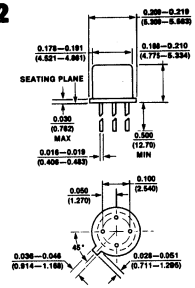
*JEDEC Registered Valve

SCHEMATIC DIAGRAM



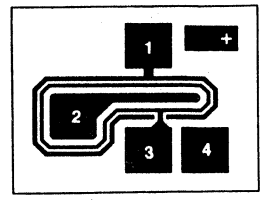
Body Internally connected to Case.
Diode protection on 2N7105/2N7107/2N7109

PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters).

CHIP CONFIGURATION



PAD
1 – Source
2 – Drain
3 – Gate
4 – Diode

For SD211/213/215 CHP, bond Gate and Diode to common point. Body is backside contact.
Dimensions: .022x.025x.013 Inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER		2N7104, 2N7105			2N7106, 2N7107			2N7108, 2N7109			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	30	35								V	I_D = 10μA V_{GS} = V_{BS} = 0	
2				10	25		10	25		20	25			I_D = 10nA V_{GS} = V_{BS} = -5V	
3		I_{DSS}	Zero Gate Voltage Drain Current			10*							μA	V_{DS} = 30V V_{GS} = V_{GS} = 0	
4		BV_{SD}	Source-Drain Breakdown Voltage	10			10			20			V	I_S = 10nA V_{GD} = V_{BD} = -5.0V	
5		BV_{DB}	Drain-Substrate Breakdown Voltage	15			15			25				I_D = 10nA, V_{GB} = 0 Source OPEN	
6		BV_{SB}	Source-Substrate Breakdown Voltage	15			15			25				I_S = 10μA, V_{GB} = 0 Drain OPEN	
7		$I_{D(off)}$	Drain-Source OFF Current			10*			10*				nA	V_{DS} = 10V	V_{GS} = V_{BS} = -5V
8												10*		V_{DS} = 20V	
9						5.0*			5.0*				μA	V_{DS} = 10V	V_{GS} = V_{BS} = -5V T_A = +125°C
10												5.0*		V_{DS} = 20V	
11		$I_{S(off)}$	Source-Drain OFF Current			10*			10*				nA	V_{SD} = 10V	V_{GD} = V_{BD} = -5V
12												10*		V_{SD} = 20V	
13						5.0*			5.0*				μA	V_{SD} = 10V	V_{GD} = V_{BD} = -5V T_A=+125°C
14												5.0*		V_{SD} = 20V	
15		I_{GSS}	Gate Reverse Current 2N7104			0.1*							nA	V_{GS} = 12V	V_{DS}= V_{BS} = 0
16			2N7106						0.1*						
17			2N7108									0.1*			
18			2N7105			1.0*							μA	V_{GS} = 25V	
19			2N7107						1.0*						
20			2N7109									1.0*		V_{GS} = 30V	
21			2N7104			1.0*							μA	V_{GS}= 12V	V_{DS} = V_{BS} = 0 T_A=+125°C
22			2N7106						1.0*						
23			2N7108									1.0*			
24			2N7105			100*								V_{GS}=25V	
25			2N7107						100*						
26			2N7109									100*		V_{GS} = 30V	
27		$V_{GS(th)}$	Gate Threshold Voltage	0.5*	1.0	2.0*	0.1*	1.0	2.0*	0.1*	1.0	2.0*	V	V_{DS} = V_{GS}, I_D = 1μA, V_{SB} = 0	
28		$r_{DS(on)}$	Drain-Source ON Resistance		50	70*		50	70*		50	70*	ohms	V_{GS}=5V	I_D = 1mA
29					30	45		30	45		30	45		V_{GS}=10V	V_{SB} = 0

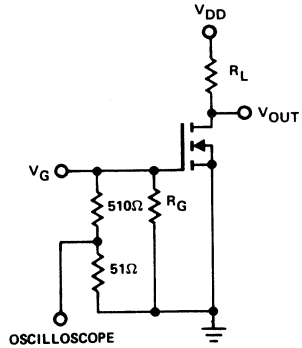
*JEDEC Registered Value

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted), continued

#		PARAMETER		2N7104, 2N7105			2N7106, 2N7107			2N7108, 2N7109			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
30		g_{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, V_{SB} = 0
31	DYNAMIC	C_{iss}	Input Capacitance		2.4	3.5*		2.4	3.5*		2.4	3.5	pF	V_{DS} = 10V V_{GS} = V_{BS} = −15V f = 1MHz
32		$C_{(gd+db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5		
33		$C_{(gs+sb)}$	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0		
34		C_{rss}	Reverse Transfer Capacitance		0.3	0.5*		0.3	0.5*		0.3	0.5*		
35		$t_{d(on)}$	Turn ON Delay Time		0.7	1.0*		0.7	1.0*		0.7	1.0*	nSec	V_{DD} = 5V, $V_{G(on)}$ = 5V R_L = 680Ω, R_G = 51Ω
36		t_r	Rise Time		0.8	1.0*		0.8	1.0*		0.8	1.0*		
37		t_{off}	Turn OFF Time		10			10			10			

*JEDEC Registered Valve

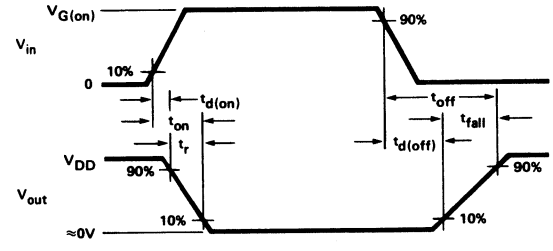
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

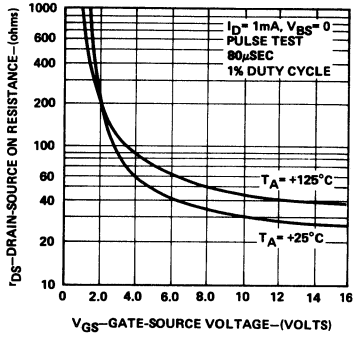
SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS

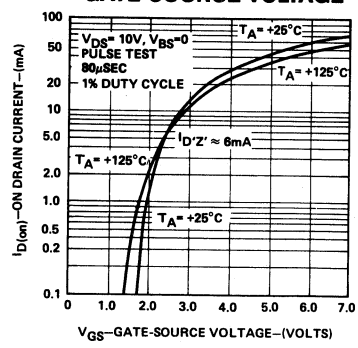


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

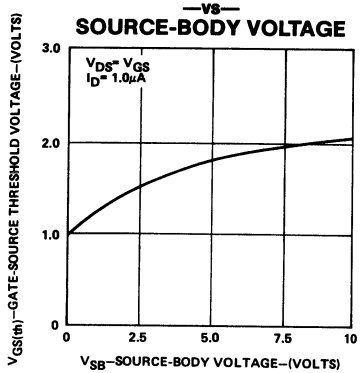
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



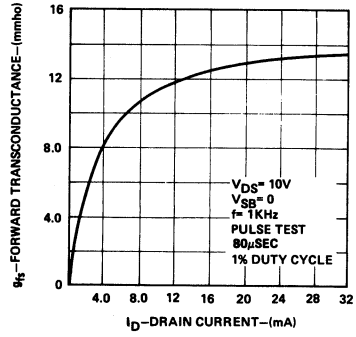
ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



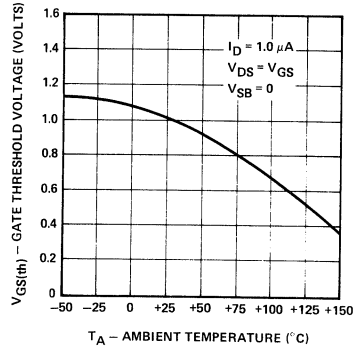
GATE-SOURCE THRESHOLD VOLTAGE —vs— SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



GATE THRESHOLD VOLTAGE —VS— AMBIENT TEMPERATURE



TOPAZ SEMICONDUCTOR

AN0110N, AN0120N AN0130N, AN0140N

N-CHANNEL ENHANCEMENT MODE D-MOS FETs 8-CHANNEL ARRAYS

ORDERING INFORMATION

18 Pin Plastic DIP	AN0110NA	AN0120NA	AN0130NA	AN0140NA
Description (each channel)	100V,100Ω	200V,300Ω	300V,300Ω	400V,350Ω

FEATURES

- Ultra-Low Channel OFF Leakage, <800pA
- High Channel-to-Channel Isolation
- 100V to 400V Capability
- Industry Standard Pin-Out

APPLICATIONS

- Electrostatic Array Drivers
- Electroluminescent Panel Drivers
- Converters
- Multi-Channel Array Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C per channel unless otherwise specified)

Drain-Source Voltage
- AN0110N ..... +100V
- AN0120N ..... +200V
- AN0130N ..... +300V
- AN0140N ..... +400V

Drain-Gate Voltage (V_{GS} = 0)
- AN0110N ..... +100V
- AN0120N ..... +200V
- AN0130N ..... +300V
- AN0140N ..... +400V

Channel-to-Channel Isolation Voltage
Drain-to-Drain Voltage (V_{GS} = 0)
- AN0110N ..... +100V
- AN0120N ..... +200V
- AN0130N ..... +300V
- AN0140N ..... +400V

Gate-Source Voltage ..... ±30V

Operating and Storage Temperature Range ..... -55 to +85°C

Lead Temperature (1/16" from mounting Surface for 10 sec.) ..... +300°C

Continuous Drain Current, Total Package

	T_A = +25°C	T_C = +25°C
AN0110N	80mA	140mA
AN0120N,AN0130N	50mA	80mA
AN0140N	40mA	75mA

Continuous Drain Current, Single Channel

	T_A = +25°C	T_C = +25°C
AN0110N	50mA	100mA
AN0120N,AN0130N	30mA	60mA
AN0140N	25mA	50mA

Continuous Device Dissipation

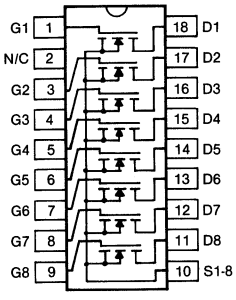
	T_A = +25°C	T_C = +25°C
Total Package	.64W	2.0W
Single Channel	.30W	1.0W

Linear Derating Factor

	T_A = +25°C	T_C = +25°C
Total Package	10.67mW/°C	33.2mW/°C
Single Channel	5mW/°C	16.6mW/°C

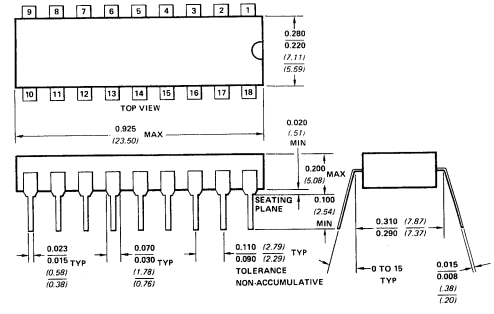
PIN CONFIGURATION & SCHEMATIC DIAGRAM

TOP VIEW



PACKAGE DIMENSIONS

18-Pin Plastic DIP

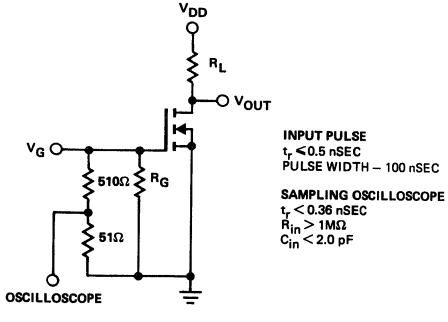


ELECTRICAL CHARACTERISTICS (T_A = +25°C per channel unless otherwise noted)

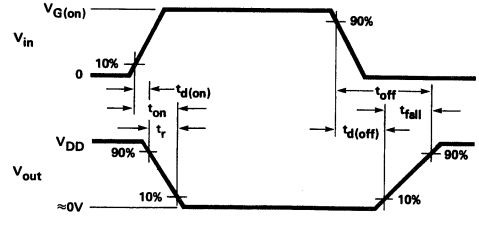
#		CHARACTERISTIC			MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	AN0110	100	160		V	I_D = 100μA, V_{GS} = 0
2				AN0120	200	300			
3				AN0130	300	400			
4				AN0140	400	450			
5		I_{DSS}	Drain-Source OFF Leakage Current	AN0110			5.0	nA	V_{DS} = 80V, V_{GS} = 0 (NOTE 1)
6				AN0120			5.0		
7				AN0120			5.0		V_{DS} = 100V, V_{GS} = 0 (NOTE 1)
8				AN0140			5.0		
9		I_{GBS}	Gate-Body Leakage Current				10	nA	V_{GS} = 20V, V_{DS} = 0
10		$V_{GS(th)}$	Gate-Source Threshold Voltage		2.0		5.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
11		$r_{DS(on)}$	Drain-Source ON Resistance	AN0110		60	100	ohms	I_D = 10mA, V_{GS} = 10V
12				AN0120		210	300		
13				AN0130		260	300		
14				AN0140		325	350		
15		$I_{D(on)}$	Drain-Source ON Current	AN0110	50			mA	V_{DS} = 25V, V_{GS} = 10V
16				AN0120	25				
17				AN0130	25				
18				AN0140	25				
19	DYNAMIC	g_{fs}	Common-Source Forward Transcond	AN0110	8.0			mmhos	V_{DS} = 25V, I_D = 10mA, f = 1KHz
20				AN0120	4.0				
21				AN0130	4.0				
22				AN0140	4.0				
23		C_{iss}	Common-Source Input Capacitance			8.0	10	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz
24		C_{oss}	Common-Source Output Capacitance			1.5	2.0		
25		C_{rss}	Common-Source Reverse Transfer Capacitance			0.8	1.0		
26		$t_{d(on)}$	Turn-ON Delay Time			3		nS	V_{DD} = 25V, $V_{G(on)}$ = 10V, R_L = 820Ω R_G = 51Ω
27		t_r	Rise Time			3			
28		$t_{d(off)}$	Turn-OFF Delay Time			5			
29		t_f	Fall Time			5			

Note 1: Limit is OFF leakage of all 8 segments in parallel.

SWITCHING TIMES TEST CIRCUIT

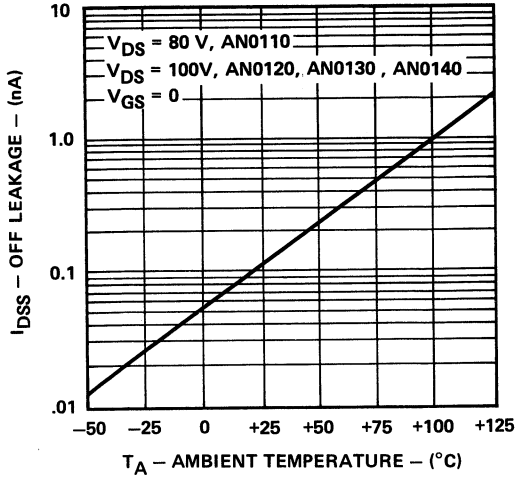


TEST WAVEFORMS

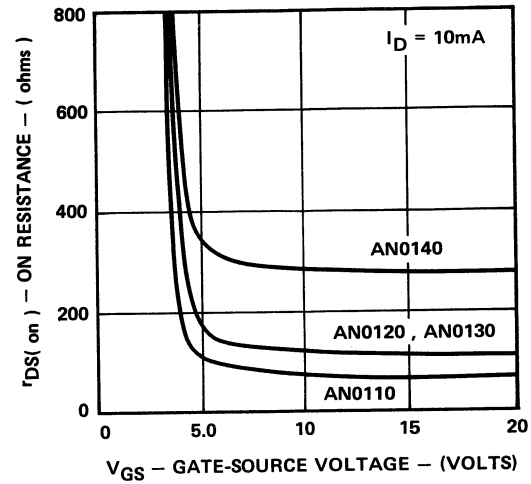


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

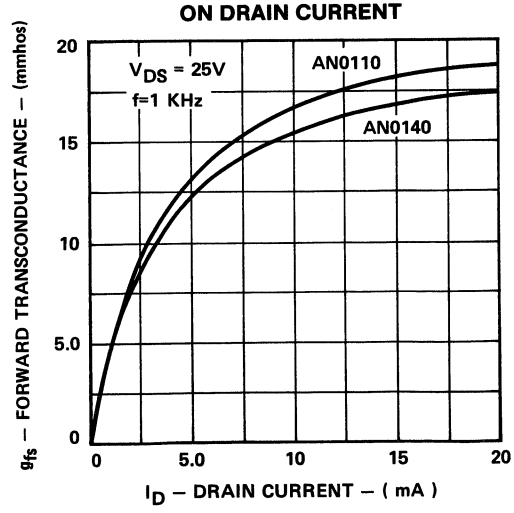
DRAIN-SOURCE OFF LEAKAGE —VS— AMBIENT TEMPERATURE



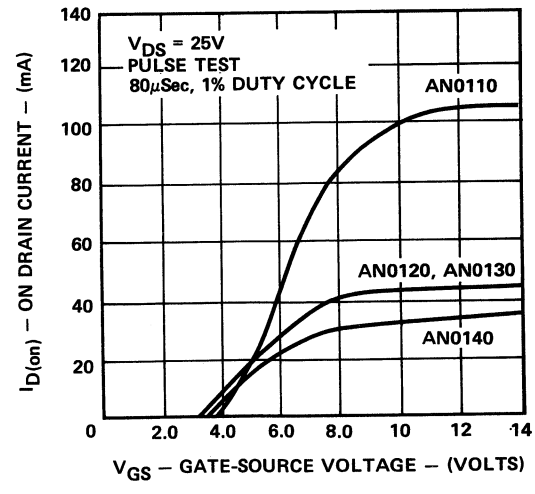
DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

AP0120N, AP0130N, AP0140N

P-CHANNEL ENHANCEMENT MODE D-MOS FETs 8-CHANNEL ARRAYS

ORDERING INFORMATION

18 Pin Plastic DIP	AP0120NA	AP0130NA	AP0140NA
Description (each channel)	-200V, 600Ω	-300V, 600Ω	-400V, 700Ω

FEATURES

- Ultra-Low Channel OFF Leakage, <-800pA
- High Channel-to-Channel Isolation
- N-Channel Complements available
- Industry Standard Pin-Out

APPLICATIONS

- Electrostatic Array Drivers
- Electroluminescent Panel Drivers
- Converters
- Multi-Channel Array Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C per channel, unless otherwise specified)

Drain-Source Voltage
- AP0120N ..... -200V
- AP0130N ..... -300V
- AP0140N ..... -400V

Drain-Gate Voltage (V_{GS} = 0)
- AP0120N ..... -200V
- AP0130N ..... -300V
- AP0140N ..... -400V

Channel-to-Channel Isolation Voltage
- Drain-to-Drain Voltage (V_{GS} = 0)
- AP0120N ..... -200V
- AP0130N ..... -300V
- AP0140N ..... -400V

Gate-Source Voltage ..... ±40V

Operating and Storage Temperature Range ..... -55 to +85°C

Lead Temperature (1/16" from mounting Surface for 10 sec.) ..... +300°C

Continuous Drain Current, Total Package

	T_A = +25°C	T_C = +25°C
AP0120N, AP0130N	-25mA	-40mA
AP0140N	-20mA	-35mA

Continuous Drain Current, Single Channel

	T_A = +25°C	T_C = +25°C
AP0120N, AP0130N, AP0140N	-15mA	-25mA

Continuous Device Dissipation

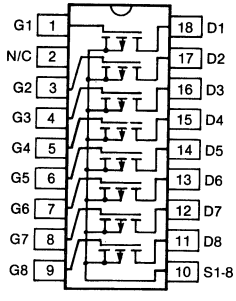
	T_A = +25°C	T_C = +25°C
Total Package	.64W	2.0W
Single Channel	.30W	1.0W

Linear Derating Factor

	T_A = +25°C	T_C = +25°C
Total Package	10.67mW/°C	33.2mW/°C
Single Channel	5mW/°C	16.6mW/°C

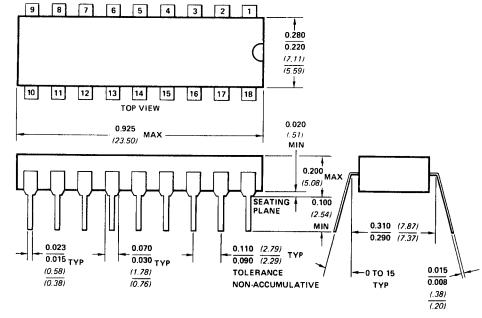
PIN CONFIGURATION & SCHEMATIC DIAGRAM

TOP VIEW



PACKAGE DIMENSIONS

18-Pin Plastic DIP



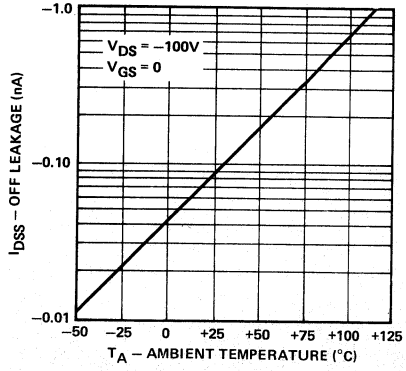
ELECTRICAL CHARACTERISTICS (T_A = +25°C per channel unless otherwise noted)

#		CHARACTERISTIC			MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	AP0120N	-200			V	I_D=-100μA, V_{GS} = 0
2				AP0130N	-300				
3				AP0140N	-400				
4		I_{DSS}	Drain-Source OFF Leakage Current				-5.0	nA	V_{DS} = -100V, V_{GS} = 0 (NOTE 1)
5		I_{GBS}	Gate-Body Leakage Current				±10	nA	V_{GB} = ±20V, V_{DS} = 0
6							±1.0	μA	V_{GB} = ±40V, V_{DS} = 0
7		$V_{GS(th)}$	Gate-Source Threshold Voltage		-2.0		-5.0	V	V_{DS} = V_{GS}, I_D = -0.5mA
8		$r_{DS(on)}$	Drain-Source ON Resistance	AP0120N, AP0130N			600	ohms	I_D = -10mA, V_{GS} = -10V
9				AP0140N			700		
10		$I_{D(on)}$	Drain-Source ON Current		-15			mA	V_{DS} = -25V,V_{GS} = -10V
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance		3.0			mmhos	V_{DS} = -25V, I_D = -5mA f = 1KHz
12		C_{iss}	Common-Source Input Capacitance			8.0	10	pF	V_{DS} = -25V, V_{GS} = 0, f = 1MHz
13		C_{oss}	Common-Source Output Capacitance			1.5	2.0		
14			Common-Source Reverse Transfer Capacitance			0.8	1.0		
15		$t_{d(on)}$	Turn-ON Delay Time			6		nS	V_{DD} = -25V, $V_{G(on)}$ = -10V R_L = 500Ω R_G = 51Ω
16		t_r	Rise time			6			
17		$t_{d(off)}$	Turn-OFF Delay Time			8			
18		t_f	Fall Time			6			

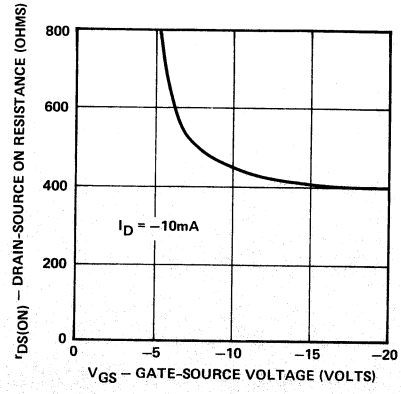
Note 1: Limit is OFF leakage of all 8 segments in parallel.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

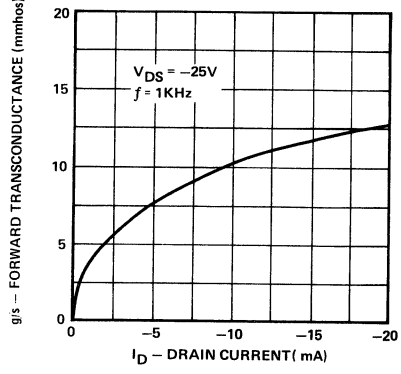
DRAIN-SOURCE OFF LEAKAGE —vs— AMBIENT TEMPERATURE



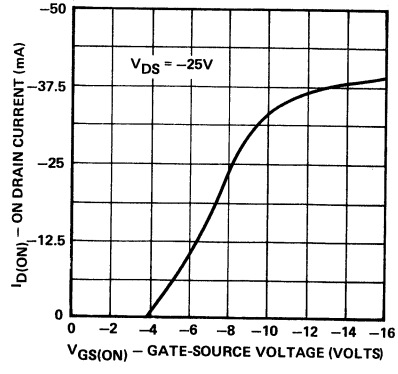
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

SD200, SD201 SD202, SD203

N-CHANNEL ENHANCEMENT-MODE LATERAL D-MOS FETs

FEATURES

- High Gain—8.0dB min. @ 1GHz
- Low Noise—5.0dB max. @ 1GHz SD202, SD203
- Low Interelectrode Capacitances

APPLICATIONS

- High-Gain VHF/UHF Amplifiers, Oscillators, and Mixers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

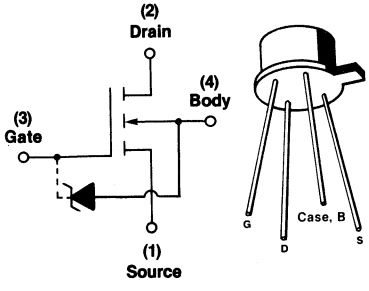
PARAMETER	SD200	SD201	SD202	SD203	UNIT
Breakdown Voltages					
V_{DS}	+25	+25	+20	+20	Vdc
V_{DB}	+25	+25	+20	+20	Vdc
V_{GS}	±40	−0.3	±40	−0.3	Vdc
		+20		+20	Vdc
V_{GB}	±40	−0.3	±40	−0.3	Vdc
		+20		+20	Vdc
V_{GD}	±40	−0.3	±40	+0.3	Vdc
		+20		+20	Vdc

I_D	Continuous Drain Current	50mA
P_T	Power Dissipation (at or below T_C = +25°C)	1.8W
	Linear Derating Factor	18 mW/°C
P_D	Power Dissipation (at or below T_A = +25°C)	360mW
	Linear Derating Factor	3.6 mW/°C
T_j	Operating Junction Temperature Range	−55 to +125°C
T_s	Storage Temperature Range	−65 to +175°C

ORDERING INFORMATION

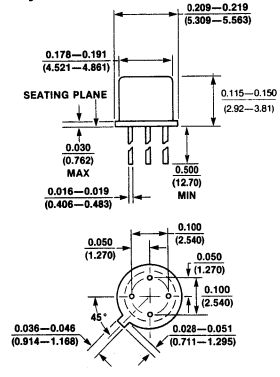
TO-52, 4 Lead Pkg.	SD200DC	SD201DC	SD202DC	SD203DC
Shorting Rings	SD200DC/R	SD201DC/R	SD202DC/R	SD203DC/R
Sorted Chips in Carriers	SD200CHP	SD201CHP	SD202CHP	SD203CHP

SCHEMATIC DIAGRAM

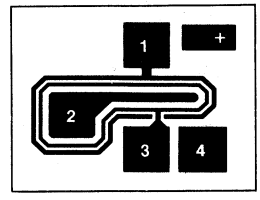


Body internally connected to Case.
Diode protection on SD201/SD203 only.

PACKAGE DIMENSIONS TO-52, 4-LEAD



CHIP CONFIGURATION



PAD
1—Source
2—Drain
3—Gate
4—Diode

For SD201-203CHP bond Gate and Diode to common point. Body is backside contact. Dimensions: .022 x .025 x .013 inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER		SD200, SD201			SD202, SD203			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage		25	30		20	25		V	I_D = 1.0μA, V_{GS} = V_{BS} = 0	
2		BV_{DB} Drain-Substrate Breakdown Voltage		25			20				I_D = 1.0μA, V_{GB} = 0 Source OPEN	
3		$I_{D(off)}$ Drain-Source OFF Current				1.0				μA	V_{DS} = 25V	V_{GS} = V_{BS} = 0
4									1.0		V_{DS} = 20V	
5		I_{GBS} Gate-Body Leakage Current	SD200			±0.1						V_{DB} = V_{SB} = 0
6			SD202						±0.1	nA	V_{GB} = ±40V	
7			SD201			1.0						
8			SD203						1.0	μA	V_{GB} = 20V	
9		$V_{GS(th)}$ Gate Threshold Voltage		0.1	1.0	2.0	0.1	1.0	2.0	V	V_{DS} = V_{GS}, I_D = 1μA, V_{SB} = 0	
10		$r_{DS(on)}$ Drain-Source ON Resistance			40	70		35	50	ohms	V_{GS} = 5V I_D = 1mA V_{SB} = 0	
11	DYNAMIC	g_{fs} Common-Source Forward Transcond.		13	14		17	20		mmhos	I_D = 20mA V_{DS} = 15V f = 1KHz, V_{SB} = 0	
12		c_{iss} Common-Source Input Capacitance			2.4	3.0		3.0	3.6	pF	I_D = 20mA	V_{DS} = 15V f = 1MHz V_{SB} = 0
13		c_{oss} Common-Source Output Capacitance			1.0	1.2		1.0	1.2		V_{GS} = 0	
14		c_{rss} Common-Source Reverse Transfer Capacitance			0.2	0.3		0.2	0.3			
15		G_{ps} Common-Source Power Gain		8.0	10		8.0	10		dB		V_{DS} = 15V f = 1GHz I_D = 20mA V_{SB} = 0
16		NF Noise Figure			4.5	6.0		4.0	5.0	dB		
17		P_i Interept Point			29			29		dBM	Δf = 2MHz	

TOPAZ SEMICONDUCTOR

SD205

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- Low Capacitance—c_{iss} 11pF typ.
- Inherently Temperature Stable by Design
- TTL Logic Compatible Input—$V_{GS(th)}$ 2.0V (max)

APPLICATIONS

- Broadband RF Power Amplifiers
- High Speed Switches and Drivers
- Pulse Amplifiers and Logic Buffers
- CMOS and TTL to High Current Interface

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

V_{DS}	Drain-Source Voltage	+25V
V_{DG}	Drain-Gate Voltage	+25V
V_{GS}	Gate-Source (Forward) Voltage	+20V
	Gate-Source (Reverse) Voltage	-0.3V
I_D	Continuous Drain Current (Note 1)	0.3A
	Continuous Drain Current (Note 2)	0.7A
	Peak Pulsed Drain Current	1.0A
P_D	Continuous Power Dissipation	
	T_A = +25°C (Note 1, Note 3)	1.0W
	T_C = +25°C (Note 1, Note 4)	6.25W
	Power Derating Factors (Note 1)	
	Free Air	10mW/°C
	Infinite Heat Sink	62.5mW/°C

Thermal Resistance (Note 1)

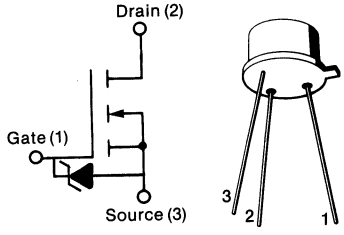
O_{ja}	Junction to Ambient	100°C/W
O_{jc}	Junction to Case	16°C/W
T_{op}	Operating Junction Temperature Range	-55 to +125°C
T_{stg}	Storage Temperature Range	-55 to +150°C

Note 1: Not applicable to chips. Final value depends on mounting.
Note 2: Pulse Test 80μSec, 1% Duty Cycle
Note 3: Free Air
Note 4: Infinite Heat Sink

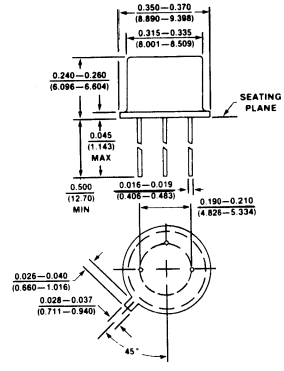
ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD205CHP
TO-39 Package	SD205HD
Description	6.0 ohm, 25V

SCHEMATIC DIAGRAM

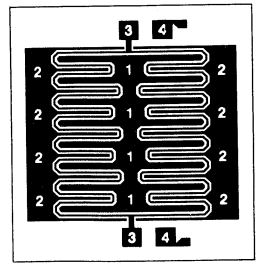


PACKAGE DIMENSIONS TO-39



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate 4—Diode
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

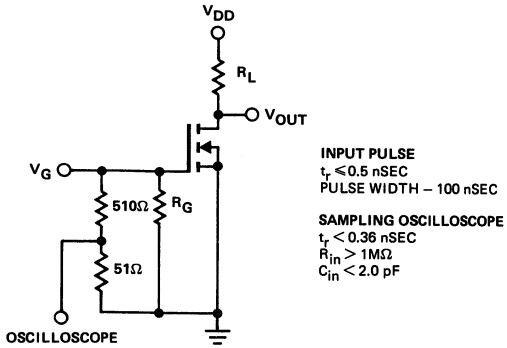
Size: .040 x .044 x .013 inch.
Body (Substrate) is backside contact.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

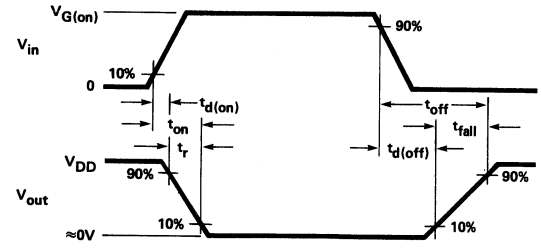
#		CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	25			V	I_D = 1.0μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5		2.0	V	I_D = 10μA, V_{DS} = V_{GS}
3	STATIC	$I_{D(on)}$ Drain-Source ON Current	1.0			μA	V_{DS} = 10V, V_{GS} = 10V (Note 1)
4	STATIC	I_{DSS} Drain-Source OFF Leakage Current			1.0	μA	V_{DS} = 25V, V_{GS} = 0
5	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance			8.0	ohms	V_{GS} = 5V, I_D = 50mA (Note 1)
6	STATIC				6.0		V_{GS} = 10V, I_D = 50mA (Note 1)
7	STATIC				6.0		V_{GS} = 10V, I_D = 500mA (Note 1)
8	STATIC	I_{GSS} Gate Body Leakage Current			1.0	μA	V_{GS} = 20V, V_{DS} = 0
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance	100			mmhos	V_{DS} = 15V, I_D = 200mA f = 1KHz (Note 1)
10	DYNAMIC	C_{iss} Common-Source Input Capacitance		11	13	pF	V_{DS} = 10V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	C_{oss} Common-Source Output Capacitance			8.0	pF	
12	DYNAMIC	C_{rss} Common-Source Reverse Transfer Capacitance			3.0	pF	
13	DYNAMIC	$t_{d(on)}$ Turn-On Delay Time		<1.0	2.0	nS	V_{DD} = 10V, $V_{G(on)}$ = 10V R_L = 133Ω, R_G = 51Ω
14	DYNAMIC	t_r Rise Time		1.0	3.0	nS	
15	DYNAMIC	t_{off} Turn-off Time		3.0	5.0	nS	
16	DYNAMIC	NF Common-Source Noise Figure			4.5	dB	V_{DS} = 10V, I_D = 100mA f = 300MHz
17	DYNAMIC	G_{PS} Common-Source Power Gain	9.0			dB	

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

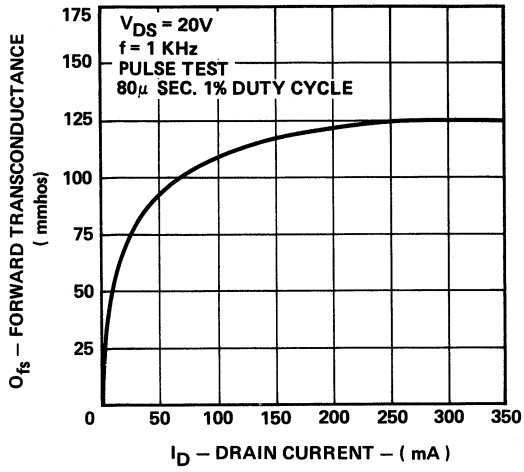


TEST WAVEFORMS

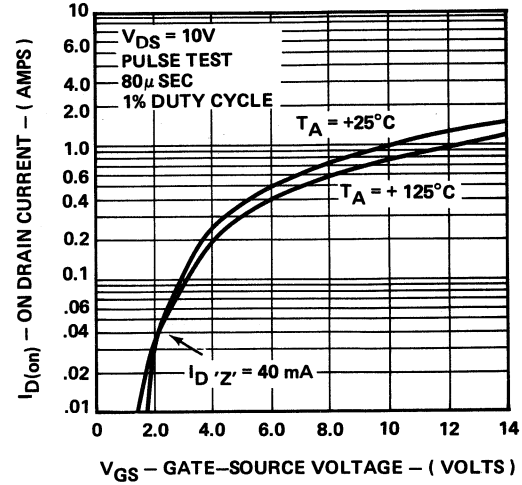


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

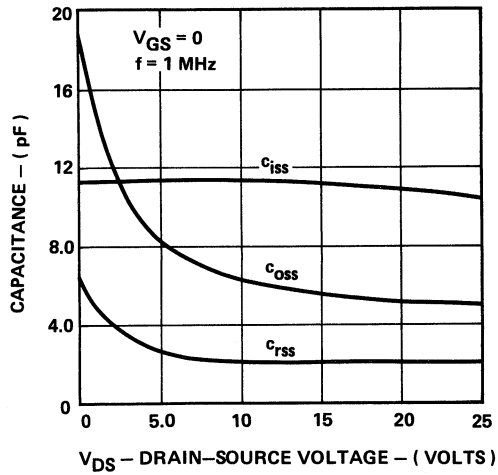
FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



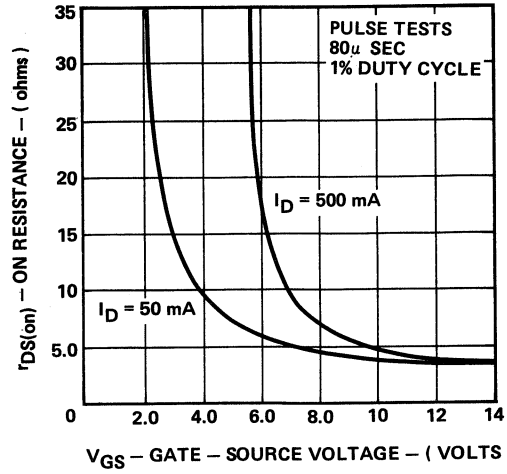
ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



CAPACITANCES —VS— DRAIN-SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

SD210, SD211, SD212, SD213, SD214, SD215

N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

APPLICATIONS

- +30V Switch Drivers—SD210, SD211
- ±10V Analog Switches—SD214, SD215
- ±5V Analog Switches—SD212, SD213

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

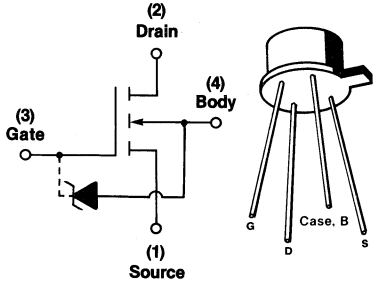
PARAMETER	SD210	SD211	SD212	SD213	SD214	SD215	UNIT
Breakdown Voltages							
V_{DS}	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	+30	+30	+15	+15	+25	+25	Vdc
V_{SB}	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	±40	−15	±40	−15	±40	−25	Vdc
		+25		+25		+30	Vdc
V_{GB}	±40	−0.3	±40	−0.3	±40	−0.3	Vdc
		+25		+25		+30	Vdc
V_{GD}	±40	−30	±40	−15	±40	−25	Vdc
		+25		+25		+30	Vdc

I_D	Continuous Drain Current	50mA
P_T	Power Dissipation (at or below T_C = +25°C)	1.2W
	Linear Derating Factor	12mW/°C
P_D	Power Dissipation (at or below T_A = +25°C)	300mW
	Linear Derating Factor	3.0mW/°C
T_j	Operating Junction Temperature Range	−55 to +125°C
T_s	Storage Temperature Range	−65 to +175°C

ORDERING INFORMATION

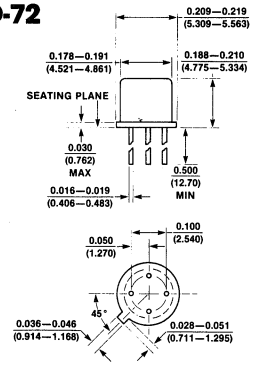
TO-72 Package	SD210DE	SD211DE	SD212DE	SD213DE	SD214DE	SD215DE
Shorting Rings	SD210DE/R	SD211DE/R	SD212DE/R	SD213DE/R	SD214DE/R	SD215DE/R
Sorted Chips in Carriers	SD210CHP	SD211CHP	SD212CHP	SD213CHP	SD214CHP	SD215CHP

SCHEMATIC DIAGRAM



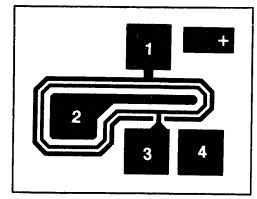
Body internally connected to Case.
Diode protection on SD211/SD213/SD215 only.

PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters).

CHIP CONFIGURATION



PAD
1—Source
2—Drain
3—Gate
4—Diode

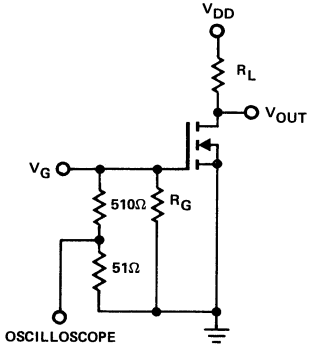
For SD211/213/R15CHP bond Gate and Diode to common point. Body is backside contact.
Dimensions: .022x.025x.013 inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER		SD210, SD211			SD212, SD213			SD214, SD215			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage		30	35								V	I_D = 10μA V_{GS} = V_{BS} = 0	
2				10	25		10	25		20	25		V	I_D = 10nA V_{GS} = V_{BS} = −5V	
3		BV_{SD} Source-Drain Breakdown Voltage		10			10			20			V	I_S = 10nA V_{GD} = V_{BD} = −5V	
4		BV_{DB} Drain-Substrate Breakdown Voltage		15			15			25			V	I_D = 10nA, V_{GB} = 0 Source OPEN	
5		BV_{SB} Source-Substrate Breakdown Voltage		15			15			25			V	I_S = 10μA, V_{GB} = 0 Drain OPEN	
6		$I_{D(off)}$ Drain-Source OFF Current				10			10				nA	V_{DS} = 10V	V_{GS} = V_{BS} = −5V
7												10	nA	V_{DS} = 20V	
8		$I_{S(off)}$ Source-Drain OFF Current				10			10				nA	V_{SD} = 10V	V_{GD} = V_{BD} = −5V
9												10	nA	V_{SD} = 20V	
10		I_{GBS} Gate-Body Leakage Current	SD210			0.1							nA	V_{GB} = ±40V	V_{DB} = V_{SB} = 0
11			SD212						0.1				nA		
12			SD214									0.1	nA		
13			SD211			10							μA		
14			SD213						10				μA	V_{GB} = 25V	
15			SD215									10	μA	V_{GB} = 30V	
16		$V_{GS(th)}$ Gate Threshold Voltage		0.5	1.0	2.0	0.1		2.0	0.1	1.0	2.0	V	V_{DS} = V_{GS}, I_D = 1μA, V_{SB} = 0	
17		$r_{DS(on)}$ Drain-Source ON Resistance			50	70		50	70		50	70	ohms	V_{GS} = 5V	I_D = 1mA
18					30	45		30	45		30	45	ohms	V_{GS} = 10V	V_{SB} = 0
19	DYNAMIC	g_{fs} Common-Source Forward Transcond.		10	12		10	12		10	12		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, V_{SB} = 0	
20		$C_{(gs + gd + gb)}$ Gate Node Capacitance			2.4	3.5		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V V_{GS} = V_{BS} = −15V f = 1MHz	
21		$C_{(gd + db)}$ Drain Node Capacitance			1.3	1.5		1.3	1.5		1.3	1.5	pF		
22		$C_{(gs + sb)}$ Source Node Capacitance			3.5	4.0		3.5	4.0		3.5	4.0	pF		
23		$C_{(dg)}$ Reverse Transfer Capacitance			0.3	0.5		0.3	0.5		0.3	0.5	pF		
24		$t_{d(on)}$ Turn ON Delay Time			0.7	1.0		0.7	1.0		0.7	1.0	nSec	V_{DD} = 5V, $V_{G(on)}$ = 10V R_L = 680Ω, R_G = 51Ω	
25		t_r Rise Time			0.8	1.0		0.8	1.0		0.8	1.0			
26		t_{off} Turn OFF Time			10			10			10				

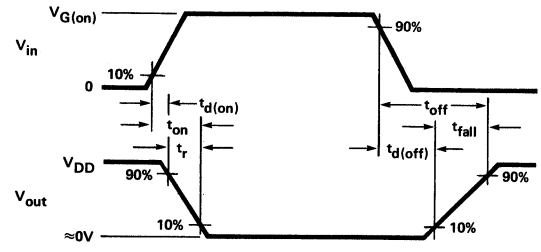
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

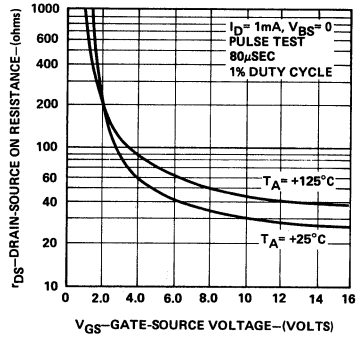
SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS

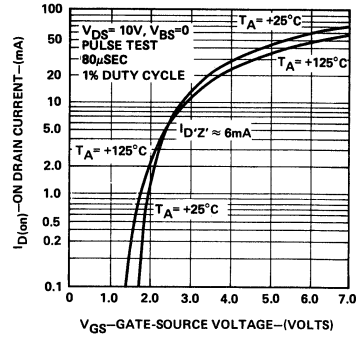


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

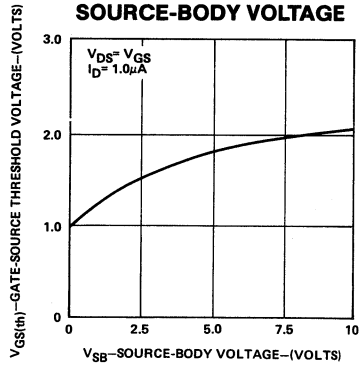
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



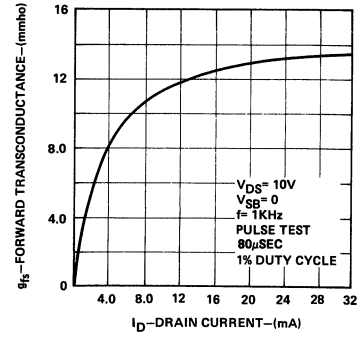
ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE —vs— SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD211A, SD215A

N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

TO-72 Package	SD211ADE	SD215ADE
Shorting Rings	SD211ADE/R	SD215ADE/R
Chips in Waffle Pack	SD211ACHP	SD215ACHP
Description	BV_{SD} 10V (min.)	BV_{SD} 20V (min.)

FEATURES

- High Input to Output Isolation — 120dB typical
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances
- Low Gamma Process
- On Resistance Guaranteed in Analog Switch Configuration

APPLICATIONS

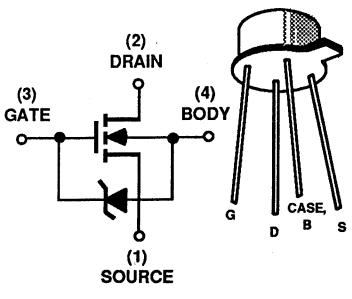
- +30V Switch Driver — SD211A
- ±10V Analog Switch — SD215A
- ±5V Analog Switch — SD211A

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD211A	SD215A	UNIT
Breakdown Voltages			
V_{DS}	+30	+20	V
V_{SD}	+10	+20	V
V_{DB}	+30	+25	V
V_{SB}	+15	+25	V
V_{GS}	–15	–25	V
	+25	+30	V
V_{GB}	–0.3	–0.3	V
	+25	+30	V
V_{GD}	–30	–25	V
	+25	+30	V

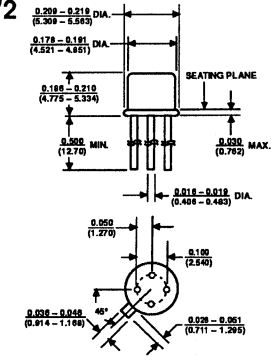
I_D	Continuous Drain Current	50mA
P_T	Power Dissipation (@ or below T_C = +25°C)	1.2W
	Linear Derating Factor	12mW/°C
P_D	Power Dissipation (@ or below T_A = +25°C)	300mW
	Linear Derating Factor	3.0mW/°C
T_j	Operating Junction Temperature Range	–55°C to +125°C
T_s	Storage Temperature Range	–65°C to +175°C

SCHEMATIC DIAGRAM



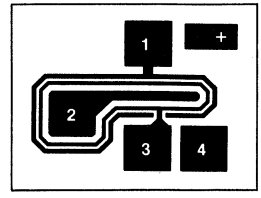
Body Internally connected to Case.

PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters).

CHIP CONFIGURATION



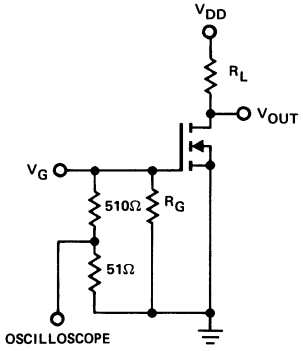
PAD
1 – Source
2 – Drain
3 – Gate
4 – Diode

Dimensions: 0.022 x 0.025 x 0.013 inches

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER		SD211A			SD215A			UNIT	TEST CONDITIONS
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	30	35					V	I_D = 10μA, V_{GS}= V_{BS} = 0
2				10	25		20	25		V	I_D= 10nA, V_{GS} = V_{BS} = –5V
3		BV_{SD}	Source-Drain Breakdown Voltage	10			20			V	I_S= 10nA, V_{GD} = V_{BD} = –5V
4		BV_{DB}	Drain-Substrate Breakdown Voltage	15			25			V	I_D = 10nA, V_{GB} = 0 Source OPEN
5		BV_{SB}	Source-Substrate Breakdown Voltage	15			25			V	I_S= 10μA, V_{GB} = 0 Drain OPEN
6		$I_{D(off)}$	Drain-Source Off Current			10				nA	V_{DS}=10V, V_{GS} = V_{BS} = –5V
7									10	nA	V_{DS} = 20V
8		$I_{S(off)}$	Source-Drain Off Current			10				nA	V_{SD} = 10V, V_{GD}= V_{BD} = –5V
9									10	nA	V_{SD} = 20V
10		I_{GBS}	Gate-Body Leakage Current			10				μA	V_{GB}= 25V, V_{DB}= V_{SB} = 0
11									10		V_{GB} = 30V
12		$V_{GS(th)}$	Gate Threshold Voltage	0.75	1.0	1.5	0.75	1.0	1.5	V	V_{DS} = V_{GS}, I_D = 1.0μA V_{SB} = 0
13		$r_{DS(on)}$	Drain-Source On Resistance			70				ohms	V_{GS} = 4.5V, I_D = 1mA V_{SB}= 5V
14									70		V_{GS} = 4.5V, I_D = 1mA V_{SB} = 10V
15					30	45		30	45		V_{GS} = 10V, I_D = 1mA V_{SB}= 0
16	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	10	13		10	13		mmhos	V_{DS}= 10V, I_D = 20mA f = 1kHz, V_{SB} = 0
17		$c_{(gs+gd+gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5	pF	V_{DS}= 10V, V_{GS} = V_{BS} = –15V, f = 1MHz
18		$c_{(gd+db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5	pF	
19		$c_{(gs+sb)}$	Source Node Capacitance		3.5	4.0		3.5	4.0	pF	
20		$c_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5	pF	
21		$t_{D(on)}$	Turn ON Delay Time		0.7	1.0		0.7	1.0	nsec	V_{DD} = 5V, $V_{G(on)}$ = 10V, R_L = 680Ω, R_G = 51Ω
22		t_r	Rise Time		0.8	1.0		0.8	1.0		
23		t_{off}	Turn OFF Time		10			10			

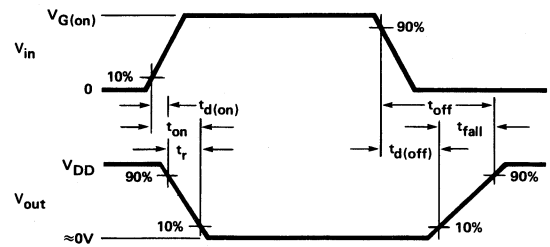
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

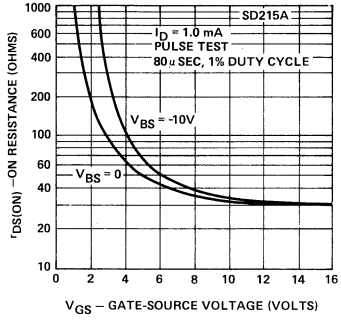
SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS

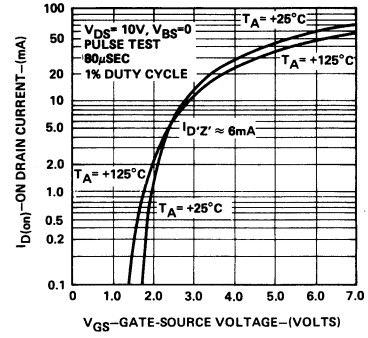


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

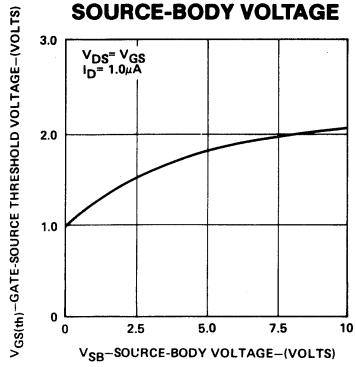
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



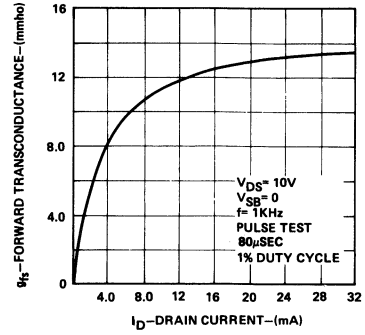
ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE —vs— SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD217, SD219

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

ORDERING INFORMATION

TO-72 Package	SD217DE	SD219DE
Shorting Ring	SD217DE/R	SD219DE/R
Sorted Chips in Waffle Pack	SD217CHP	SD219CHP
Description	6.0 ohm, 25V V_{SB} = 15V min	6.0 ohm, 25V V_{SB} = 20V min

FEATURES

- CMOS Compatible Input
- Small Package, Standard Pin-Out
- TTL and CMOS Compatible Input
- Low Capacitance
- Peak Pulsed Current, 1 Amp min

APPLICATIONS

- ± 10V Analog Switch, SD219DE
- ± 7.5 Analog Switch, SD217DE
- High Speed, Medium Power, Switch Drivers
- Sample and Hold and Track and Hold
- A-to-D and D-to-A Converters

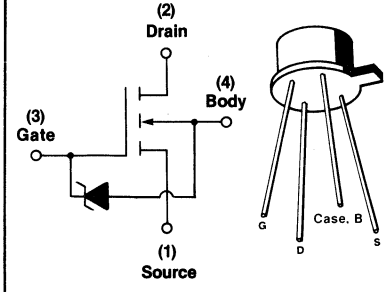
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

V_{DS} Drain-Source Voltage ..... +25V
V_{DB} Drain-Body Voltage
SD217 ..... +22.5V
SD219 ..... +25V
V_{SD} Source-Drain Voltage
SD217 ..... +15V
SD219 ..... +20V
V_{SB} Source-Body Voltage
SD217 ..... +22.5V
SD219 ..... +25V
V_{GB} Gate-Body Voltage ..... +30V
V_{GS} Gate-Source Voltage ..... ±22.5V
V_{GD} Gate-Drain Voltage ..... ±22.5V
I_D Peak Pulsed Drain Current ..... +1.0A

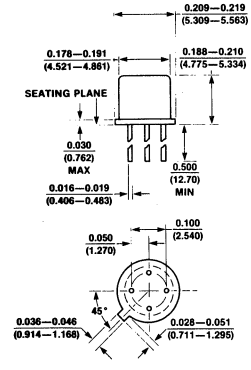
I_D Continuous Drain Current (Note 1) 160mA
P_D Continuous Power Dissipation (Note 1)
T_A = +25°C (Free Air) 300mW
T_C = +25°C (Infinite Heat Sink) 1.2W
Power Derating Factors (Note 1)
Free Air ..... 3.0mW/°C
Infinite Heat Sink ..... 12mW/°C
Thermal Resistance (Note 1)
O_{ja} Junction to Ambient ..... 333°C/W
O_{jc} Junction to Case ..... 83°C/W
T_{op} Operating Junction Temperature Range ..... -55 to +125°C
T_{stg} Storage Temperature Range ..... -55 to +150°C

Note 1: Not applicable to chips. Final value depends on mounting.

SCHEMATIC DIAGRAM

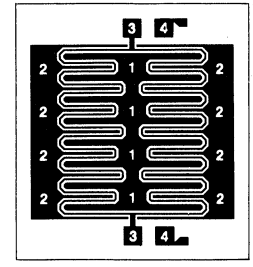


PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate 4—Diode
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

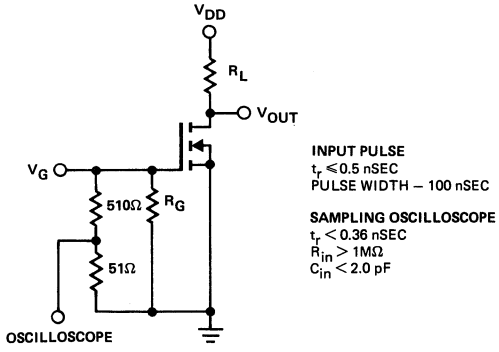
Size: .040 x .044 x .013 inch.
Body (Substrate) is backside contact.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

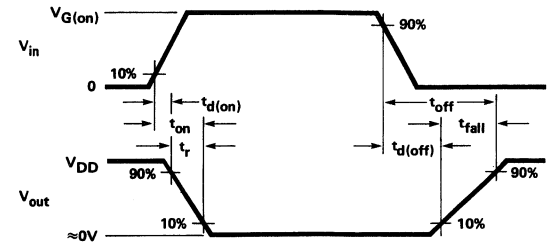
#		CHARACTERISTIC			MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage		25	30		V	$I_D = 10\mu A$, $V_{GS} = V_{BS} = 0$	
2					15	20			$I_D = 100nA$, $V_{GS} = V_{BS} = -5V$	
3		BV_{SD}	Source-Drain Breakdown Voltage	SD217	15			V	$I_S = 100nA$, $V_{GD} = V_{BD} = -5V$	
4				SD219	20					
5		BV_{DB}	Drain-Body Breakdown Voltage	SD217	22.5			V	$I_D = 100nA$, $V_{GB} = 0$, Source Open	
6				SD219	25					
7		BV_{SB}	Source-Body Breakdown Voltage	SD217	22.5			V	$I_S = 100nA$, $V_{GB} = 0$, Drain Open	
8				SD219	25					
9		$I_{D(off)}$	Drain-Source OFF Leakage Current				100	nA	$V_{DS} = 15V$, $V_{GS} = V_{BS} = -5V$	
10		$I_{S(off)}$	Source-Drain OFF Leakage Current				100		$V_{SD} = 15V$, $V_{GD} = V_{BD} = -5V$	
11		I_{GB}	Gate-Body ON Leakage Current				10	μA	$V_{GB} = 30V$, $V_{GS} = V_{GD} = 22.5V$	
12		$V_{GS(th)}$	Gate-Source Threshold Voltage		0.1		2.0	V	$V_{DS} = V_{GS}$, $I_D = 10\mu A$, $V_{SB} = 0$	
13		$I_{D(on)}$	Drain-Source ON Current (Note 1)		1.0			A	$V_{DS} = V_{GS} = 10V$, $V_{SB} = 0$	
14		$r_{DS(on)}$	Drain-Source ON Resistance (Note 1)				8.0	ohms	$V_{GS} = 5.0V$	$I_D = 50mA$, $V_{SB} = 0$
15							6.0		$V_{GS} = 10V$	
16							6.0			$I_D = 500mA$, $V_{SB} = 0$
17	DYNAMIC	g_{fs}	Common-Source (Note 1) Forward Transconductance		100			mmhos	$V_{DS} = 15V$, $I_D = 200mA$, $V_{SB} = 0$, F = 1KHz	
18		$C_{(gs+gd+gb)}$	Gate Node Capacitance				30	pF	$V_{DS} = 10V$, $V_{GS} V_{BS} = -15V$, f = 1MHz	
19		$C_{(gd+db)}$	Drain-Node Capacitance				15			
20		$C_{(gs+sb)}$	Source Node Capacitance				40			
21		$C_{(dg)}$	Reverse Transfer Capacitance				5.0			
22		t_{on}	Turn ON Time			2.0	4.0	nS	V_{DD}= 10V, $V_{G(on)}$ = 10V, R_L= 133Ω, R_G= 51Ω	
23		t_{off}	Turn OFF Time			3.0	5.0			

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

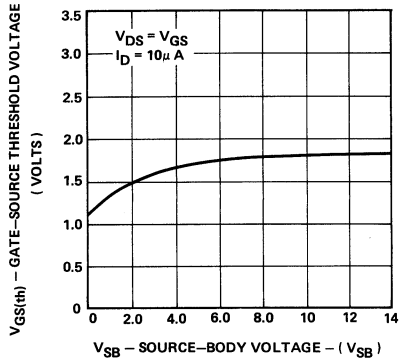


TEST WAVEFORMS

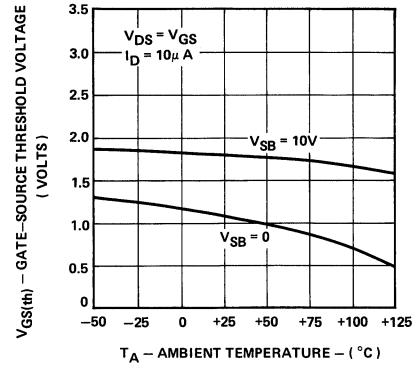


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

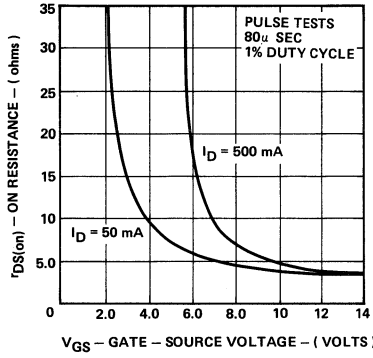
GATE-SOURCE THRESHOLD VOLTAGE —VS— SOURCE-BODY VOLTAGE



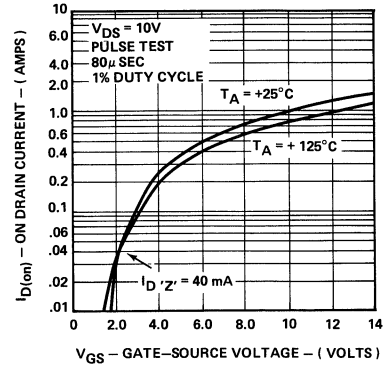
GATE-SOURCE THRESHOLD VOLTAGE —VS— TEMPERATURE



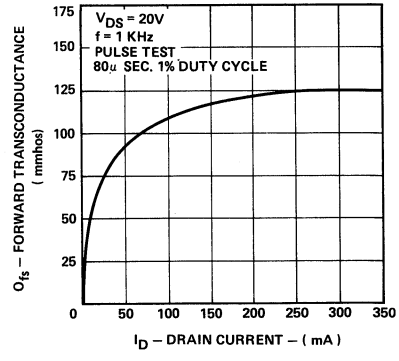
DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD220

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD220CHP
TO-39 Hermetic Package	SD220HD
Description	60V, 9.0 ohm

FEATURES

- Low Capacitance—C_{iss} 12pF, C_{rss} 0.6pF—(typ)
- Fast Switching
- TTL Logic Compatible Input—$V_{GS(th)}$ 2.3V (max)

APPLICATIONS

- Broadband RF Power Amplifiers
- High Speed Switch Drivers
- Pulse Amplifiers and Logic Buffers
- CMOS and TTL to High Current Interfaces

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

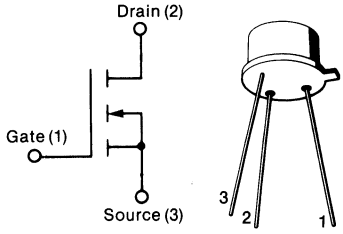
V_{DS} Drain-Source Voltage ..... +60V
V_{DG} Drain-Gate (Forward) Voltage ..... +60V
Drain-Gate (Reverse) Voltage ..... -30V
V_{GS} Gate-Source (Forward) Voltage ..... +30V
Gate-Source (Reverse) Voltage ..... -30V
I_D Continuous Drain Current 230mA
Pulsed Drain Current (Note 1) 800mA
P_D Continuous Device Dissipation
T_A = +25°C (Note 2) 1.0W
T_C = +25°C (Note 3) 6.25W

Power Derating Factors
Free Air ..... 10mW/°C
Infinite Heat Sink ..... 62.5mW/°C

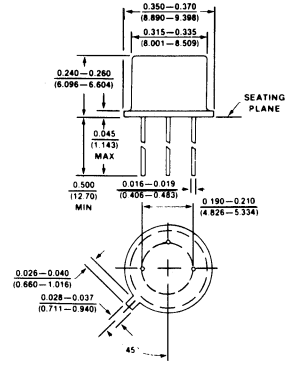
Thermal Resistance
ϕ_{ja} Junction to Ambient ..... 100°C/W
ϕ_{jc} Junction to Case ..... 16°C/W
T_{op} Operating Junction Temperature Range ..... -55 to +125°C
T_{stg} Storage Temperature Range ..... -55 to +150°C

Note 1: Pulse Test 80μSec, 1% Duty Cycle **Note 2:** Free Air **Note 3:** Infinite Heat Sink

SCHEMATIC DIAGRAM

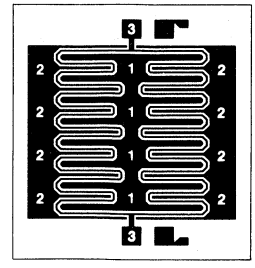


PACKAGE DIMENSIONS TO-39



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate.

Size: .040 x .044 x .013 inch.
Body (Substrate) is backside contact.

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD220 MIN	SD220 TYP	SD220 MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60	100		V	I_D = 1.0μA, V_{GS} = 0	
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	0.1	0.8	2.3		I_D = 10μA, V_{DS} = V_{GS}	
3				0.5	1.5	3.0		I_D = 1mA, V_{DS} = V_{GS}	
4		$I_{D(on)}$	ON Drain Current	500			mA	V_{DS} = 6V	V_{GS} = 10V (Note 1)
5				600	700			V_{DS} = 10V	
6		I_{DSS}	Drain-Source OFF Leakage Current		0.1	1.0	μA	V_{DS} = 60V, V_{GS} = 0	
7		$r_{DS(on)}$	Drain-Source ON Resistance		7.5	10	ohms	V_{GS} = 5V	I_D = 50mA (Note 1)
8					6.5	9.0		V_{GS} = 10V	
9					9.0	12			I_D = 500mA (Note 1)
10		I_{GSS}	Gate Leakage Currents			±1.0	nA	V_{GS} = ±20V, V_{DS} = 0	
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	150	190		mmhos	V_{DS} = 30V, I_D = 300mA f = 1KHz (Note 1)	
12		c_{iss}	Common-Source Input Capacitance		12	15	pF	V_{DS} = 30V, V_{GS} = 0 f = 1MHz	
13		c_{oss}	Common-Source Output Capacitance		2.8	3.5			
14		c_{rss}	Common-Source Reverse Transfer Capacitance		0.6	1.0			
15		$t_{d(on)}$	Turn-On Delay Time		1.0	2.0	nS	V_{DD} = 30V $V_{G(on)}$ = 5.0V R_L = 90 ohms R_G = 51 ohms	
16		t_r	Rise Time		1.0	3.0			
17		t_f	Fall Time		3.0	5.0			

Note 1: Pulse Test 80μSec, 1% Duty Cycle

TOPAZ SEMICONDUCTOR

SD303

N-CHANNEL ENHANCEMENT-MODE DUAL GATE D-MOS FET

FEATURES

- Normally Off-Enhancement-Mode Operation
- Dual Gate with Gate Protective Diodes
- Low Feedback Capacitance — c_{rss} .02pF (typ)
- Wide Dynamic Range-Remote AGC capability
- High Power Gain- 10dB min. @ 1GHz
- Low Noise-7.0dB max. @ 1GHz
- Low Cross-Modulation Distortion

APPLICATIONS

- Wide Band (Unneutralized) VHF/UHF Amplifiers
- VHF/UHF Linear Mixers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

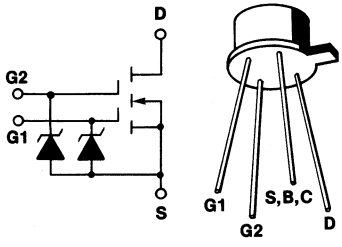
V_{DS}	Drain-Source Voltage	+20V
V_{G1B}	Gate 1-Substrate Voltage	−0.3 to +10V
V_{G2B}	Gate 2-Substrate Voltage	−0.3 to +15V
I_D	Continuous Drain Current (Note 1)	50mA
P_D	Continuous Power Dissipation (Note 1)	
	T_A = +25°C (Free Air)	360mW
	T_C = +25°C (Infinite Heat Sink)	1.8W
	Power Derating Factors (Note 1)	
	Free Air	3.6mW/°C
	Infinite Heat Sink	18mW/°C
T_{op}	Operating Junction Temperature Range	−55 to +125°C
T_{stg}	Storage Temperature Range	−65 to +175°C

Note 1: Not applicable to chips. Final value depends mounting substrate.

ORDERING INFORMATION

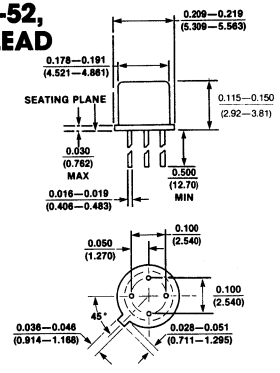
Sorted Chips in Carriers	SD303CHP
TO-52, 4 Lead Package	SD303DC
Shorting Rings	SD303DC/R

SCHEMATIC DIAGRAM



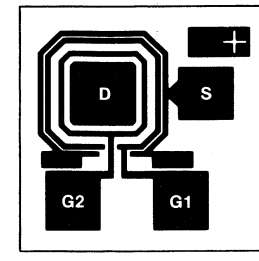
Pin 1-Drain, 2-Gate 2
Pin 3-Gate 1,
Pin 4-Source, Substrate, Case

PACKAGE DIMENSIONS TO-52, 4 LEAD



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Chip backside connected to source
Dimensions: .022 x .022 x .013 inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (TA = +25°C unless otherwise noted)

#		PARAMETER		SD303 MIN	SD303 TYP	SD303 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20	25		V	$I_D = 5\mu A$ $V_{G1S} = V_{G2S} = 0$	
2	STATIC	I_{DSS}	Drain-Source OFF Leakage Current		.01	1.0	μA	$V_{DS} = 15V$ $V_{G1S} = V_{G2S} = 0$	
3	STATIC	I_{G1SS}	Gate 1 Leakage Current		1.0	100	nA	$V_{G1S} = 5V$ $V_{G2S} = V_{DS} = 0$	
4	STATIC	I_{G2SS}	Gate 2 Leakage Current		1.0	100	nA	$V_{G2S} = 10V$ $V_{G1S} = V_{DS} = 0$	
5	STATIC	V_{T1}	Gate 1-Source Threshold Voltage	0.1	0.5	1.5	V	$V_{DS} = V_{G1S}$ $V_{G2S} = 10V$, $I_D = 1\mu A$	
6	STATIC	V_{T2}	Gate 2-Source Threshold Voltage	0.1	0.5	1.5	V	$V_{G1S} = 4V$	$V_{DS} = V_{G2S}$ $I_D = 1\mu A$
7	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		65	80	ohms	$I_D = 1mA$, $V_{G1S} = 5V$ $V_{G2S} = 10V$	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	13	15		mmhos	$V_{DS} = 15V$, $I_D = 18mA$ $V_{G2S} = 10V$, f = 1KHz	
9	DYNAMIC	c_{iss}	Common-Source Input Capacitance		3.0	3.5	pF	$V_{DS} = 15V$, $I_D = 18mA$ $V_{G2S} = 10V$, f = 1MHz	
10	DYNAMIC	c_{oss}	Common-Source Output Capacitance		0.6		pF	$V_{DS} = 15V$, $V_{G1S} = 0$ $V_{G2S} = 10V$, f = MHz	
11	DYNAMIC	c_{rss}	Common-Source Reverse Transfer Capacitance		.02		pF		
12	DYNAMIC	G_{ps}	Power Gain	10	14		dB	f = 1GHz	$V_{DS} = 15V$ $V_{G2S} = 10V$ $I_D = 18mA$
13	DYNAMIC	NF	Noise Figure		5.5	7.0	dB	f = 1GHz	
14	DYNAMIC	AGC (V_{G2S})	Range of Automatic Gain Control		40		dB	$V_{G1S} \cong 2.5V$ f = 500MHz	$V_{DS} = 15V$ $V_{G2S} = 10V$ to 0V
15	DYNAMIC	E_{INT}	Interfering Signal at Gate for 1% Cross-Modulation Distortion (Peak Voltage ref. to 300 ohm system)		150		mV	fo = 1.000GHz fi = 0.995GHz	$V_{DS} = 15V$ $V_{G2S} = 10V$ $I_D = 18mA$

TOPAZ SEMICONDUCTOR

SD304, SD306

N-CHANNEL ENHANCEMENT-MODE DUAL GATE D-MOS FET

FEATURES

- Normally Off-Enhancement-Mode Operation
- Dual Gate with Gate Protective Diodes
- Low Feedback Capacitance — C_{rss} .03pF (typ)
- Wide Dynamic Range-Remote AGC capability
- High Power Gain- 17dB min. @ 500MHz (SD306)
- Low Noise-6.0dB max. @ 500MHz (SD306)
- Low Cross-Modulation Distortion

APPLICATIONS

- Wide Band (Unneutralized) VHF/UHF Amplifiers
- VHF/UHF Linear Mixers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage
- SD304 ..... +25V
- SD306 ..... +20V

V_{G1B} Gate 1-Substrate Voltage
- SD304 ..... −0.3 to +10V
- SD306 ..... −0.3 to +20V

V_{G2B} Gate 2-Substrate Voltage
- SD304 ..... −0.3 to +15V
- SD306 ..... −0.3 to +20V

I_D Continuous Drain Current (Note 1) 50mA

P_D Continuous Power Dissipation (Note 1)
- T_A = +25°C (Free Air) 300mW
- T_C = +25°C (Infinite Heat Sink) 1.2W

Power Derating Factors (Note 1)
- Free Air ..... 3.0mW/°C
- Infinite Heat Sink ..... 12mW/°C

T_{op} Operating Junction Temperature Range ..... −55 to +125°C

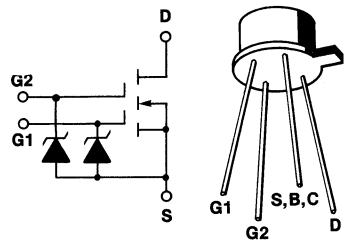
T_{stg} Storage Temperature Range .. −65 to +175°C

Note 1: Not applicable to chips. Final value depends mounting substrate.

ORDERING INFORMATION

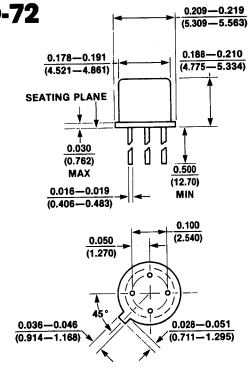
Sorted Chips in Carriers	SD304CHP	SD306CHP
TO-72 Package	SD304DE	SD306DE
Shorting Rings	SD304DE/R	SD306DE/R

SCHEMATIC DIAGRAM



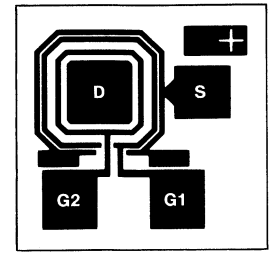
Pin 1-Drain, 2-Gate 2
Pin 3-Gate 1,
Pin 4-Source, Substrate, Case

PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Chip backside connected to source
Dimensions: .022 x .022 x .013 inches

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ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER	SD304 MIN	SD304 TYP	SD304 MAX	SD306 MIN	SD306 TYP	SD306 MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	25	30		20	25		V	I_D = 5μA $V_{G1S} = V_{G2S} = 0$
2	STATIC	I_{DSS} Drain-Source OFF Leakage Current		.01	1.0		.01	1.0	μA	V_{DS} = 15V $V_{G1S} = V_{G2S} = 0$
3	STATIC	I_{G1SS} Gate 1 Leakage Current		1.0	100		1.0	100	nA	V_{G1S} = 5V $V_{G2S} = V_{DS} = 0$
4	STATIC	I_{G2SS} Gate 2 Leakage Current		1.0	100		1.0	100	nA	V_{G2S} = 10V $V_{G1S} = V_{DS} = 0$
5	STATIC	V_{T1} Gate 1-Source Threshold Voltage	0.1	1.0	2.0	0.1	0.5	1.5	V	$V_{DS} = V_{G1S}$ V_{G2S} = 10V, I_D = 1μA
6	STATIC	V_{T2} Gate 2-Source Threshold Voltage	0.1	1.0	2.0				V	V_{G1S} = 4V; $V_{DS} = V_{G2S}$, I_D = 1μA
7	STATIC	V_{T2} Gate 2-Source Threshold Voltage				0.1	0.5	1.5	V	V_{G1S} = 5V; $V_{DS} = V_{G2S}$, I_D = 1μA
8	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		90	130		65	100	ohms	I_D = 1mA, V_{G1S} = 5V V_{G2S} = 10V
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance	8.0	10		13	15		mmhos	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 1KHz
10	DYNAMIC	c_{iss} Common-Source Input Capacitance		2.5	3.0		3.3	3.6	pF	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 1MHz
11	DYNAMIC	c_{oss} Common-Source Output Capacitance		1.0	1.2		1.0	1.3	pF	V_{DS} = 15V, V_{G1S} = 0 V_{G2S} = 10V, f = 1MHz
12	DYNAMIC	c_{rss} Common-Source Reverse Transfer Capacitance		.03			.03		pF	V_{DS} = 15V, V_{G1S} = 0 V_{G2S} = 10V, f = 1MHz
13	DYNAMIC	Re(Y11) Input Admittance					1.11		mmhos	V_{DS} = 15V, I_D = 18mA
14	DYNAMIC	Im(Y11) Input Admittance					4.76		mmhos	V_{G2S} = 10V, f = 200MHz

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

PARAMETER		SD304			SD306			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
Re (Y22)	Output Admittance					1.05		mmhos	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	
Im (Y22)						1.54		mmhos		
Re (Y21)	Forward Transmittance					13.23		mmhos		
Im (Y21)						−5.62		mmhos		
Re (Y12)	Reverse Transmittance					0.01		mmhos		
Im (Y12)						−0.04		mmhos		
G_{ps}	Power Gain	13	16					dB	f = 500MHz	V_{DS} = 15V V_{G2S} = 10V I_D = 18mA
					17	20		dB	f = 200MHz	
NF	Noise Figure		5.0	6.0				dB	f = 500MHz	
						1.5	2.5	dB	f = 200MHz	
AGC (V_{G2S})	Range of Automatic Gain Control		40					dB	V_{G1S} ≅ 3.5V f = 500MHz	V_{DS} = 15V V_{G2S} = 10V to 0V
						50		dB	V_{G1S} ≅ 2.5V f = 200MHz	
E_{INT}	Interfering Signal at Gate for 1% Cross-Modulation Distortion (Peak Voltage ref. to 50 ohm system)		200					mV	fo = 500MHz fi = 501MHz	V_{DS} = 15V V_{G2S} = 10V I_D = 18mA
						480		mV	fo = 200MHz fi = 196MHz	
G_{psc}	Conversion Power Gain (I_D = 8mA)				14	17		dB	V_{DS} = 15V, V_{G1S} = V_{G2S} frf = 200MHz, f1 = 245MHz	

TOPAZ SEMICONDUCTOR

SD411

N-CHANNEL DEPLETION-MODE DUAL D-MOS FET

FEATURES

- Normally OFF Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Pin Compatible to Industry Standard Dual J-FETs with addition of Substrate Bias Pin

APPLICATIONS

- High-Speed Analog Comparators
- Wide-Band Differential Amplifiers
- Cascode Amplifiers
- High Intercept Point Balanced Mixers

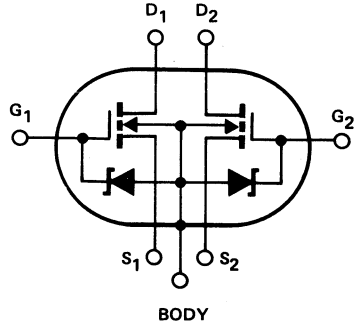
ABSOLUTE MAXIMUM RATINGS (per side, T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage	+20V
V_{SD} Source-Drain Voltage	+10V
V_{DB} Drain-Body Voltage	+25V
V_{SB} Source-Body Voltage	+15V
V_{GD} Gate-Drain Voltage	+25V
V_{GS} Gate-Source Voltage	+25V
V_{GB} Gate-Body Voltage	+25V
V_{G1G2} Gate-to-Gate Voltage	+25V
V_{D1D2} Drain-to-Drain Voltage	+20V
V_{S1S2} Source-to-Source Voltage	+15V
I_D Continuous Drain Current	+50 mA
P_D Device Dissipation (each side)	360 mW
Derating Factor	2.88 mW/°C
P_D Total Device Dissipation	500 mW
Derating Factor	4 mW/°C
T_j Operating Junction Temperature Range	-55 to +150°C
T_S Storage Temperature Range	-55 to +150°C
T_L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260°C

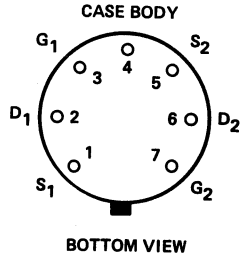
ORDERING INFORMATION

TO-78 Hermetic Package	SD411HD

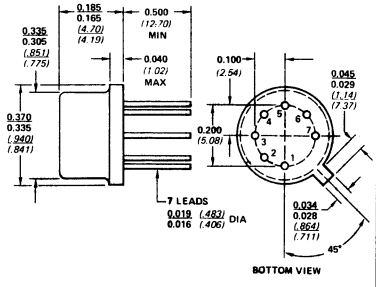
SCHEMATIC DIAGRAM



PIN CONFIGURATION



PACKAGE DIMENSIONS TO-78



All dimensions in inches and (millimeters)

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ELECTRICAL CHARACTERISTICS (T_A = +25°C, per side, unless otherwise noted)

#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DS}	Drain Source Breakdown Voltage	20			V	I_D = 10 nA, V_{GS} = V_{BS} = -5V
2		BV_{SD}	Source-Drain Breakdown Voltage	10				I_S = 10 nA, V_{GD} = V_{BD} = -5V
3		BV_{DB}	Drain-Body Breakdown Voltage	25				I_D = 10 nA, V_{GB} = 0 Source Open
4		BV_{SB}	Source-Body Breakdown Voltage	15				I_S = 10μA, V_{GB} = 0 Drain open
5		I_{DSX}	Drain-Source Leakage Current		0.7	10	nA	V_{DS} = 20V, V_{GS} = V_{BS} = -5V
6		I_{GBS}	Gate-Body Leakage Current			1.0	μA	V_{GS} = 25V, V_{DB} = V_{SB} = 0
7		$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	V	I_D = 1.0μA, V_{DS} = V_{GS}, V_{SB} = 0
8		$r_{DS(ON)}$	Drain-Source[1] ON Resistance			70	ohms	I_D = 1.0mA, V_{GS} = 5.0V, V_{SB} = 0
9	DYNAMIC	g_{fs}	Common-Source[1] Forward Transcond.	10	12		mmhos	V_{DS} = 10V, I_D = 20mA, V_{SB} = 0 f = 1KHz
10		C_{iss}	Common-Source Input Capacitance		3.5		pF	V_{DS} = 10V V_{GS} = V_{BS} = 0 f = 1MHz
11		C_{oss}	Common-Source Output Capacitance		1.2			
12		C_{rss}	Common Source Reverse Transfer Capacitance		0.3			
13		$C_{(gs + sb)}$	Source Node Capacitance		4.5			
14	MATCH	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate Source Voltage		25		mV	V_{DS} = 10V I_D = 5.0 mA V_{SB} = 0
15		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Differential Drift		25		μV/°C	T_A = -55°C to +125°C

Note 1: Pulse Test, 80μsec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS: See SD5000 Data Sheet

TOPAZ SEMICONDUCTOR

SD1100, SD1101

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETS

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

Drain-Source Voltage
- SD1100 ..... 450V
- SD1101 ..... 400V

Drain-Gate Voltage (V_{GS} = 0)
- SD1100 ..... 450V
- SD1101 ..... 400V

Gate-Source Voltage ..... ±30V

Continuous Drain Current
- SD1100DD, SD1101DD 80mA
- SD1100HD, SD1101HD 140mA

Peak Drain Current
- SD1100DD, SD1101DD 250mA
- SD1100HD, SD1101HD 300mA

Continuous Device Dissipation
- SD1100DD, SD1101DD 360mW
- SD1100HD, SD1101HD 800mA

Linear Derating Factor
- SD1100DD, SD1101DD ..... 2.9mW/°C
- SD1100HD, SD1101HD ..... 6.4mW/°C

Operating Junction Temperature Range ..... −55 to +150°C

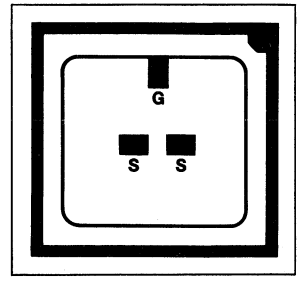
Storage Temperature Range ..... −55 to +150°C

Lead Temperature (1/16″ from mounting surface for 30 Sec) ..... +260°C

ORDERING INFORMATION

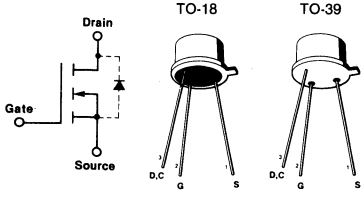
Sorted Chips in Carriers	SD1100CHP	SD1101CHP
TO-18 Package	SD1100DD	SD1101DD
TO-39 Package	SD1100HD	SD1101HD
Description	450V, 35 ohm	400V, 25 ohm

CHIP CONFIGURATION



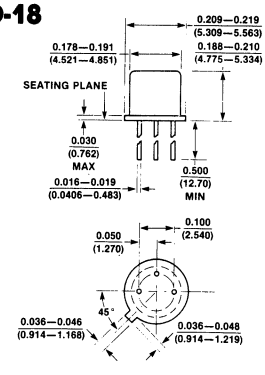
Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

SCHEMATIC DIAGRAM/ PACKAGES



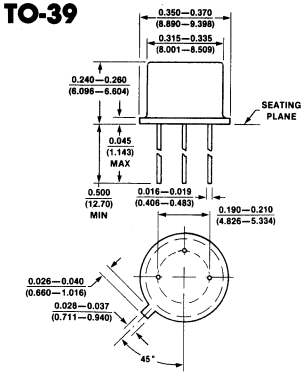
Body internaly connected to Source.
Drain common to Case.

PACKAGE DIMENSIONS TO-18



All dimensions in inches and (millimeters)

PACKAGE DIMENSIONS TO-39



All dimensions in inches and (millimeters)

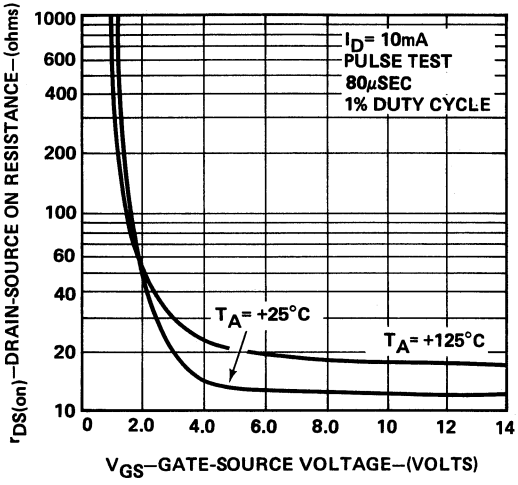
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1100			SD1101			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	450	475		400	425		V	I_D = 10 μ A, V_{GS} = 0
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	1.0	3.0	5.0	1.0	3.0	5.0	V	I_D = 10μ A, V_{DS} = V_{GS}
3		I_{GBS}	Gate-Body Leakage Current		.03	1.0		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4		I_{DSS}	Drain-Source OFF Leakage Current		2.0	200				nA	V_{DS} = 360V, V_{GS} = 0
5		I_{DSS}	Drain-Source OFF Leakage Current					2.0	200	nA	V_{DS} = 320V, V_{GS} = 0
6		$I_{D(on)}$	ON Drain Current	250	400		250	400		mA	V_{DS} = 25V, V_{GS} = 15V (Note 1)
7		$r_{DS(on)}$	Drain-Source ON Resistance		25	35		20	25	ohms	I_D = 10mA, V_{GS} = 15V
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance		210			210		mmhos	V_{DS} = 25V, I_D = 250mA f = 1KHz (Note 1)
9		c_{iss}	Common-Source Input Capacitance		80			80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
10		c_{rss}	Common-Source Reverse Transfer Capacitance		1.3			1.3			
11		c_{oss}	Common-Source Output Capacitance		10.5			10.5			

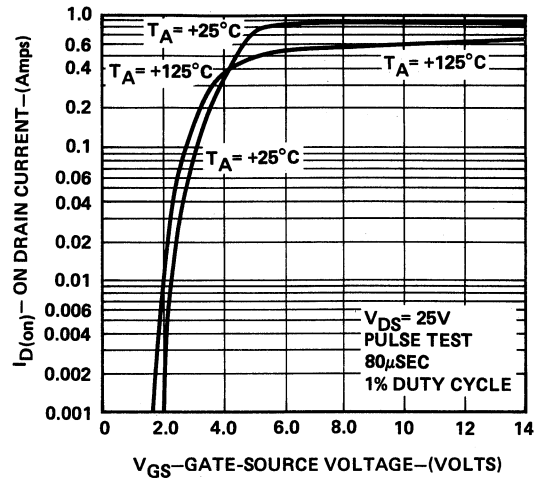
Note 1: Pulse Test 80μ Sec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

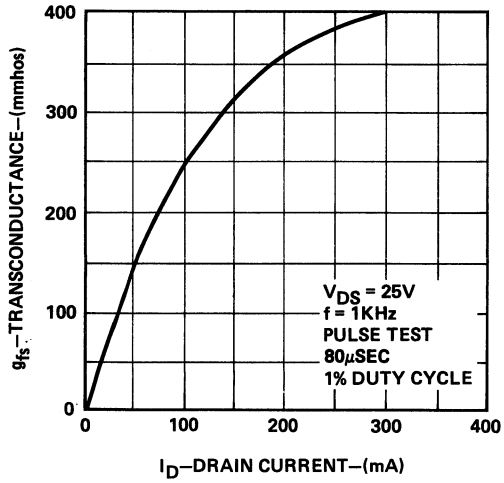
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD1102, SD1112, SD1113

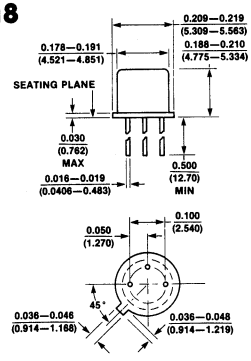
N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Carriers	SD1102CHP	SD1112CHP	SD1113CHP
TO-18 Package	SD1102DD	SD1112DD	SD1113DD
TO-39 Package	SD1102HD	SD1112HD	SD1113HD
TO-92 Package	SD1102BD	SD1112BD	SD1113BD
Description	250V, 10 ohms	200V, 7.0 ohms	200V, 10 ohms

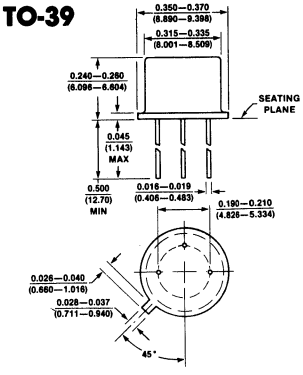
PACKAGE DIMENSIONS

TO-18



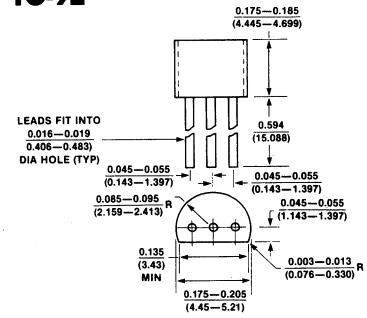
All dimensions in inches and (millimeters)

TO-39



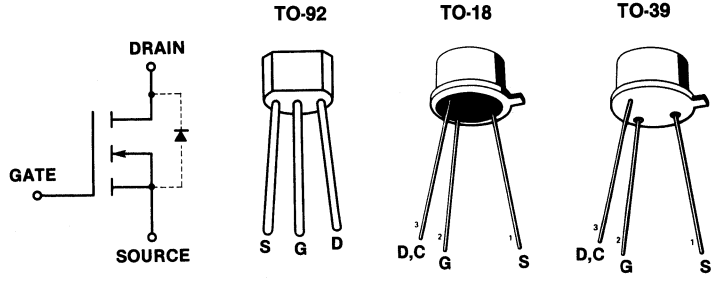
All dimensions in inches and (millimeters)

TO-92

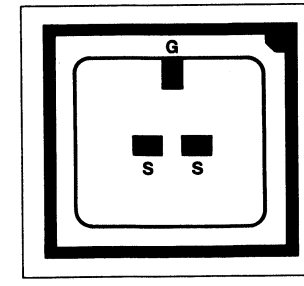


All dimensions in inches and (millimeters)

SCHEMATIC DIAGRAM/PACKAGES



CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage
- SD1102 ..... 250V
- SD1112, SD1113 ..... 200V

Drain-Gate Voltage (V_{GS} = 0)
- SD1102 ..... 250V
- SD1112, SD1113 ..... 200V

Gate-Source Voltage ..... ±30V

Continuous Drain Current

	T_A = 25°C	T_C = 25°C
SD1102BD, SD1113BD.	.13	.23A
SD1112BD	.15	.27A
SD1102DD, SD1113DD.	.14	.31A
SD1112DD	.16	.37A
SD1102HD, SD1113HD.	.23	.57A
SD1112HD	.27	.69A

Peak Pulsed Drain Current 0.5A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C	
SD1102/1112/1113BD ..	0.30	1.0	W
SD1102/1112/1113DD ..	0.36	1.8	W
SD1102/1112/1113HD ..	1.0	6.25	W

Linear Derating Factor

	T_A = + 25°C	T_C = +25°C	
SD1102/1112/1113BD ..	2.4	8.0	mW/°C
SD1102/1112/1113DD ..	2.9	14.4	mW/°C
SD1102/1112/1113HD ..	8.0	50	mW/°C

Operating Junction Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C

Lead Temperature (1/16″ from mounting surface for 30 Sec) ..... +260°C

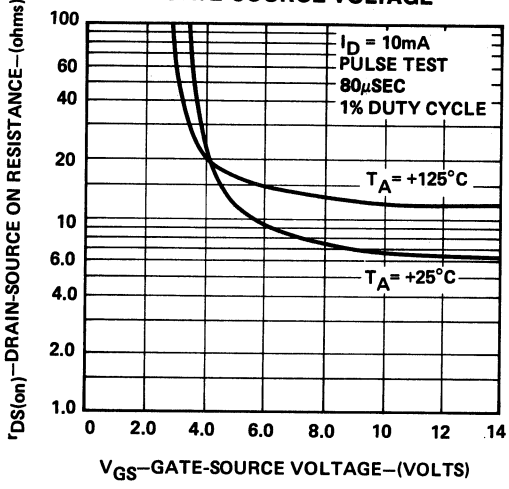
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1102 MIN	SD1102 TYP	SD1102 MAX	SD1112, SD1113 MIN	SD1112, SD1113 TYP	SD1112, SD1113 MAX	UNIT	TEST CONDITION
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage		250	270		200	250		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage		1.0	3.0	5.0	1.0	3.0	5.0	V	V_{DS} = V_{GS}, I_D = 10μA
3	STATIC	I_{GBS} Gate-Body Leakage Current			.03	1.0		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{DSS} Drain-Source OFF Leakage Current			0.1	1.0				μA	V_{DS} = 200V, V_{GS} = 0
5	STATIC	I_{DSS} Drain-Source OFF Leakage Current						0.1	1.0	μA	V_{DS} = 160V, V_{GS} = 0
6	STATIC	$I_{D(on)}$ ON Drain Current		0.5			0.5			A	V_{DS} = 25V, V_{GS} = 15V (Note 1)
7	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance	SD1102		8.0	10				ohms	I_D = 10mA, V_{GS} = 15V (Note 1)
8	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance	SD1112					6.0	7.0	ohms	I_D = 10mA, V_{GS} = 15V (Note 1)
9	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance	SD1113					7.0	10	ohms	I_D = 10mA, V_{GS} = 15V (Note 1)
10	DYNAMIC	g_{fs} Common-Source Forward Transcond.			300			300		mmhos	V_{DS} = 25V, I_D = 0.5A f = 1KHz (Note 1)
11	DYNAMIC	c_{iss} Common-Source Input Capacitance			80			80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	c_{rss} Common-Source Reverse Transfer Capacitance			1.3			1.3		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
13	DYNAMIC	c_{oss} Common-Source Output Capacitance			10.5			10.5		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz

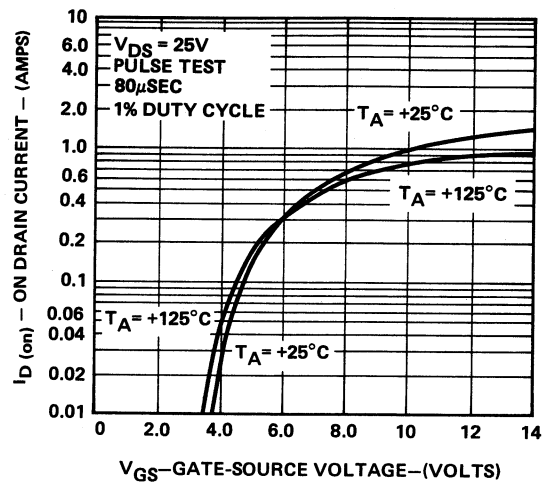
Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

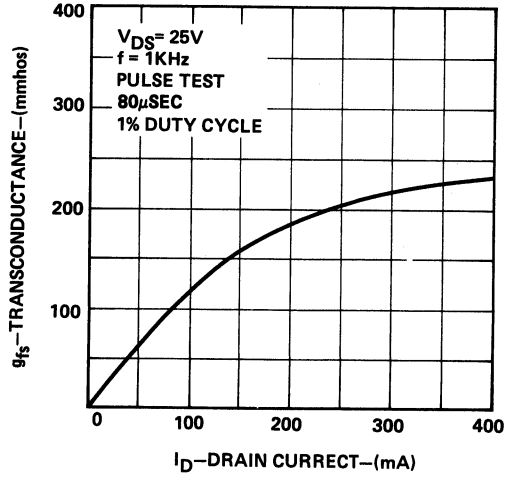
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD1106

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- **Inherent Current Sharing Capability when Paralleled**
- **Simple Straight-Forward DC Biasing**
- **Extended Safe Operating Area**
- **Inherently Temperature Stable— Output Current Decreases as Temperature Increases**

APPLICATIONS

- **High-Speed Pulse Amplifiers**
- **Logic Buffers**
- **Line Drivers**
- **Solid-State Relays**

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage 60V
Drain-Gate Voltage (V_{GS} = 0) 60V
Gate-Source Voltage ..... ±30V
Continuous Drain Current (Note 1, Note 2) . 0.5A
Peak Drain Current (Note 1, Note 2) 2.0A
Continuous Device Dissipation
(Note 1, Note 2) 1.8W
Linear Derating Factor
(Note 1, Note 2) ..... 14.4mW/°C
Operating Junction
Temperature Range ..... -55 to +150°C
Storage Temperature Range ..... -55 to +150°C
Lead Temperature (1/16" from mounting
surface for 30 Sec) ..... +260°C

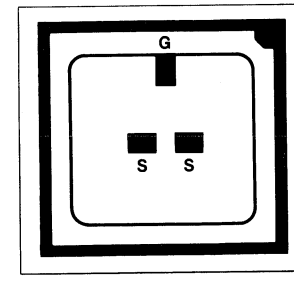
Note 1: T_{Case} = +25°C

Note 2: Not applicable to chips. Final value depends upon mounting substrate.

ORDERING INFORMATION

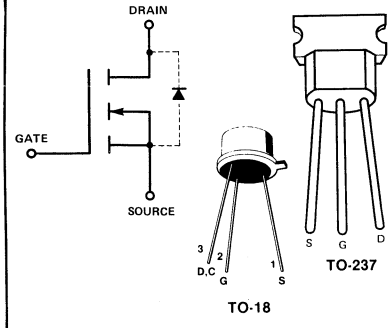
Sorted Chips in Carriers	SD1106CHP
TO-18 Package	SD1106DD
TO-237 Package	SD1106AD

CHIP CONFIGURATION



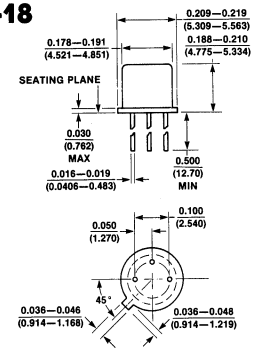
Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

SCHEMATIC DIAGRAM



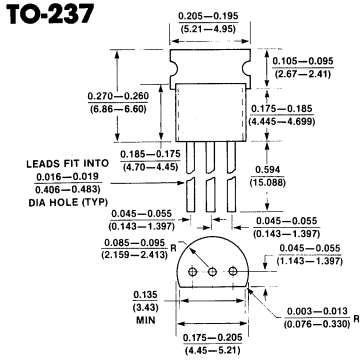
Drain common to Case or Tab.

PACKAGE DIMENSIONS TO-18



All dimensions in inches and (millimeters)

PACKAGE DIMENSIONS TO-237



All dimensions in inches and (millimeters)

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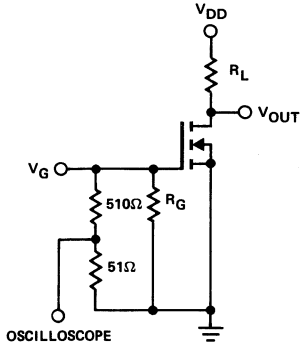
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1106 MIN	SD1106 TYP	SD1106 MAX	UNIT	TEST CONDITION
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60			V	I_D = 100μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8		2.5	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.03	10	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{DSS}	Drain-Source OFF Leakage Current		.01	10	μA	V_{DS} = 40V, V_{GS} = 0
5	STATIC	$I_{D(on)}$	ON Drain Current	0.25			A	V_{DS} = 25V (Note 1); V_{GS} = 5V
6	STATIC	$I_{D(on)}$	ON Drain Current	0.50			A	V_{DS} = 25V (Note 1); V_{GS} = 10V
7	STATIC	$V_{DS(on)}$	Drain-Source ON Voltage		1.8	2.5	V	V_{GS} = 10V, I_D = 0.5A (Note 1)
8	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	100	270		mmhos	V_{DS} = 15V, I_D = 0.5A f = 1KHz (Note 1)
9	DYNAMIC	C_{iss}	Common-Source Input Capacitance		80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
10	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.3		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	C_{oss}	Common-Source Output Capacitance		10.5		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	t_{on}	Turn-On Time		4.0	6.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohms, $V_{G(on)}$ = 10V
13	DYNAMIC	t_{off}	Turn-Off Time		4.0	6.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohms, $V_{G(on)}$ = 10V

Note 1: Pulse Test 80μSec, 1% Duty Cycle

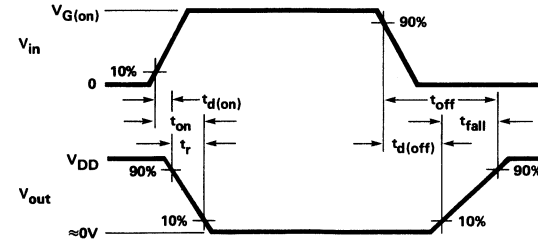
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS



TOPAZ SEMICONDUCTOR

SD1107, SD1117

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable — Output Current Decreases as Temperature Increases

APPLICATIONS

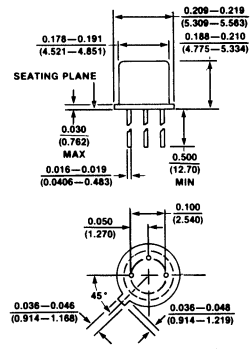
- High-Speed Pulse Amplifiers
- CMOS Logic to High-Current Interfaces
- High-Speed Switching
- Line Drivers

ORDERING INFORMATION

Sorted Chips in Carriers	SD1107CHP	SD1117CHP
TO-18 Package	SD1107DD	SD1117DD
TO-39 Package	SD1107HD	SD1117HD
TO-92 Package	SD1107BD	SD1117BD
Description	100V, 4.0 ohm	60V, 2.5 ohm

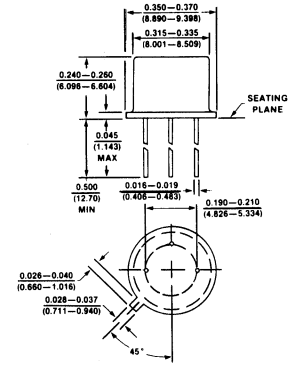
PACKAGE DIMENSIONS

TO-18



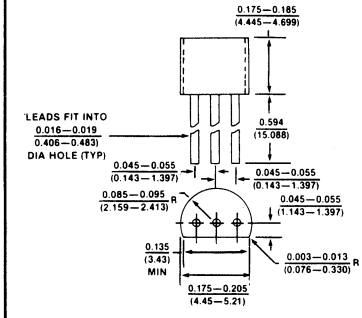
All dimensions in inches and (millimeters)

TO-39



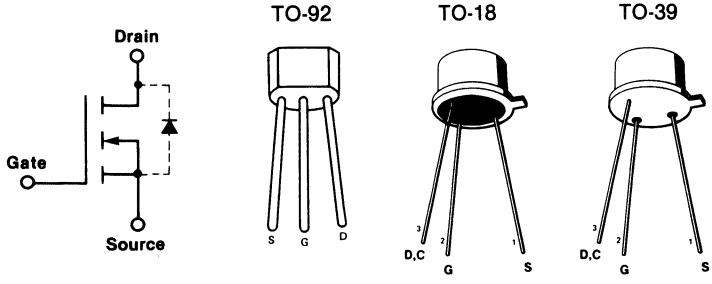
All dimensions in inches and (millimeters)

TO-92

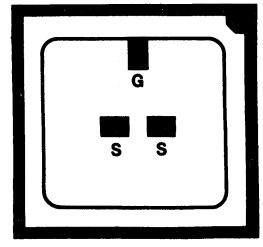


All dimensions in inches and (millimeters)

SCHEMATIC DIAGRAM/PACKAGES



CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

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TOPAZ SEMICONDUCTOR

SD1107, SD1117

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS POWER FET ARRAYS

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable — Output Current Decreases as Temperature Increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- CMOS Logic to High-Current Interfaces
- High-Speed Switching
- Line Drivers
- Stepper Motor Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage
- SD1107 ..... 100V
- SD1117 ..... 60V

Drain-Gate Voltage (V_{GS} = 0)
- SD1107 ..... 100V
- SD1117 ..... 60V

Gate-Source Voltage ..... ±30V

Continuous Drain Current

	T_A = 25°C	T_C = 25°C	
Total Package			
SD1107	.29	.51	A
SD1117	.37	.65	A
Single Device			
SD1107	.20	.36	A
SD1117	.25	.46	A

Peak Pulsed Drain Current 2.0A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C	
Total Package	.64	2.0	W
Single Device	.30	1.0	W

Linear Derating Factor

	T_A = +25°C	T_C = +25°C	
Total Package	5.1	16	mW/°C
Single Device	2.4	8.0	mW/°C

Operating Junction Temperature Range ..... −55 to +150°C

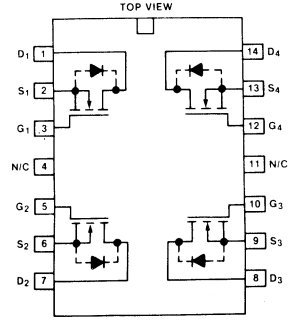
Storage Temperature Range ..... −55 to +150°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

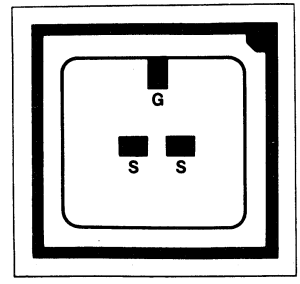
ORDERING INFORMATION

14 Pin Plastic DIP	SD1107N	SD1117N
Description	100V, 4.0 ohm	60V, 2.5 ohm

SCHEMATIC DIAGRAM

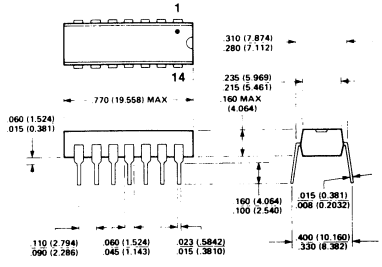


CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

PACKAGE DIMENSIONS 14 PIN DIP



All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage
- SD1107 ..... 100V
- SD1117 ..... 60V

Drain-Gate Voltage (V_{GS} = 0)
- SD1107 ..... 100V
- SD1117 ..... 60V

Gate-Source Voltage ..... ±30V

Continous Drain Current

	T_A = 25°C	T_C = 25°C
SD1107BD	.20	.36 A
SD1107DD	.22	.49 A
SD1107HD	.36	.91 A
SD1117BD	.25	.46 A
SD1117DD	.28	.62 A
SD1117HD	.46	1.15 A

Peak Pulsed Drain Current 2.0A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C	
SD1107BD, SD1117BD	0.30	1.0	W
SD1107DD, SD1117DD	0.36	1.8	W
SD1107HD, SD1117HD	1.0	6.25	W

Linear Derating Factor

	T_A = +25°C	T_C = +25°C	
SD1107BD, SD1117BD	2.4	8.0	mW/°C
SD1107DD, SD1117DD	2.9	14.4	mW/°C
SD1107HD, SD1117HD	8.0	50	mW/°C

Operating Junction Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C

Lead Temperature (1/16″ from mounting surface for 30 Sec) ..... +260°C

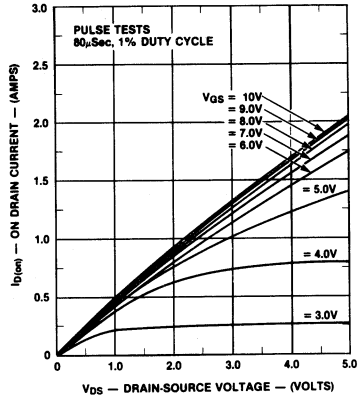
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1107 MIN	SD1107 TYP	SD1107 MAX	SD1117 MIN	SD1117 TYP	SD1117 MAX	UNIT	TEST CONDITION
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	100	140		60	90		V	I_D = 10μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 1mA
3		I_{GBS}	Gate-Body Leakage Current		.03	1.0		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4						10			10		T_A = +125°C
5		I_{DSS}	Drain-Source OFF Leakage Current		0.1	1.0				μA	V_{DS} = 80V, V_{GS} = 0
6						50					T_A = +125°C
7								0.1	1.0		V_{DS} = 48V, V_{GS} = 0
8									50		T_A = +125°C
9		$I_{D(on)}$	ON Drain Current	2.0	3.0		2.0	3.5		A	V_{DS} = 25V, V_{GS} = 10V (Note 1)
10		$r_{DS(on)}$	Drain-Source ON Resistance		3.2	5.0		2.3	4.5	ohms	V_{GS} = 5V, I_D = 0.3A (Note 1)
11					2.9	4.0		2.0	2.5		V_{GS} = 10V, I_D = 1.0A (Note 1)
12	DYNAMIC	g_{fs}	Common-Source Forward Transcond.		500			500		mmhos	V_{DS} = 25V, I_D = 1.0A, f = 1KHz (Note 1)
13		c_{iss}	Common-Source Input Capacitance		80			80		pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz
14		c_{rss}	Common-Source Reverse Transfer Capacitance		1.3			1.3			
15		c_{oss}	Common-Source Output Capacitance		10.5			10.5			
16		t_{on}	Turn-On Time		4.0	6.0		4.0	6.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohms, $V_{G(on)}$ = 10V
17		t_{off}	Turn-Off Time		4.0	6.0		4.0	6.0		

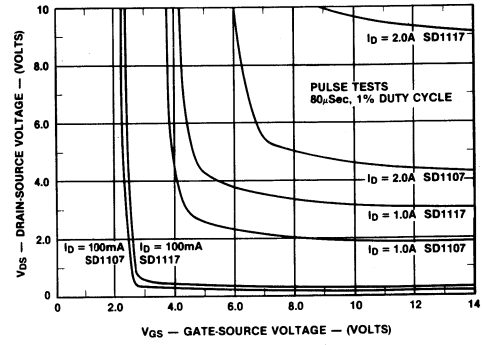
Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise noted)

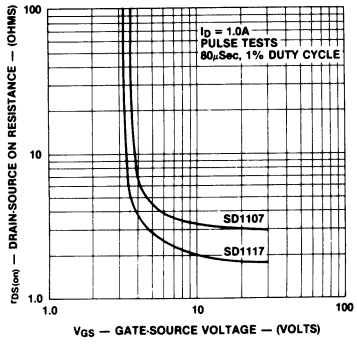
SATURATION CHARACTERISTICS
SD1117



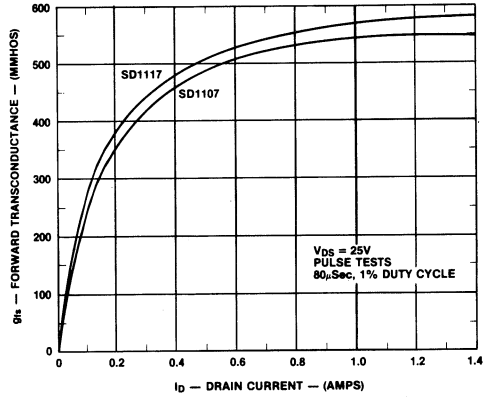
ON-VOLTAGE CHARACTERISTICS



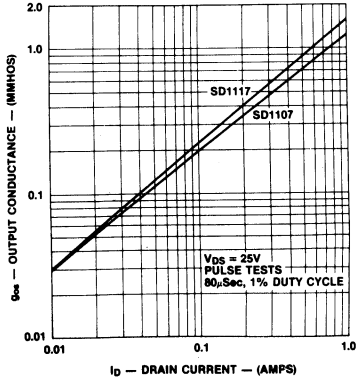
DRAIN-SOURCE ON RESISTANCE
-VS-
GATE-SOURCE VOLTAGE



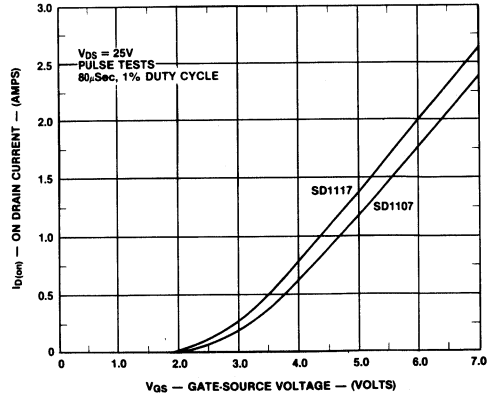
FORWARD TRANSCONDUCTANCE
-VS-
ON DRAIN CURRENT



OUTPUT CONDUCTANCE
-VS-
ON DRAIN CURRENT



TRANSFER CHARACTERISTICS



TOPAZ SEMICONDUCTOR

SD1122

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETS

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable — Output Current Decreases as Temperature Increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Line Interrupters
- Outpulser Switches
- Display Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage 200V
Drain-Gate Voltage (V_{GS} = 0) 200V
Gate-Source Voltage ..... ±30V
Continuous Device Dissipation (Note 2) 0.3W
Linear Derating Factor (Note 2) ..... 2.4mW/°C
Continuous Drain Current (Note 2) 0.12A
Peak Drain Current (Note 1, Note 2) 0.5A
Continuous Device Dissipation (Note 1, Note 2) 1.0W
Linear Derating Factor (Note 1, Note 2) ..... 8.0mW/°C
Thermal Resistance, Junction to case ..... 125°C/W
Operating Junction Temperature Range ..... −55 to +150°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (1/16″ from mounting surface for 30 Sec) ..... +260°C

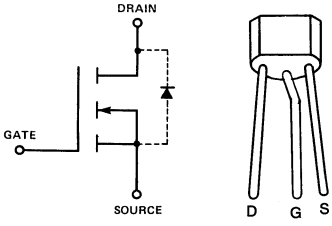
Note 1: T_{CASE} = +25°C

Note 2: Not applicable to chips. Final value depends upon mounting substrate.

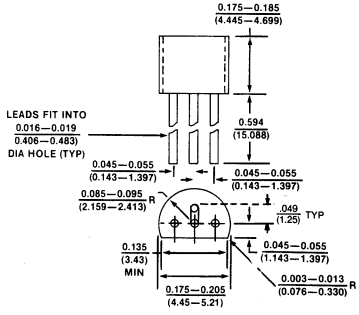
ORDERING INFORMATION

Sorted Chips in Carriers	SD1122CHP
TO-92 Pkg-Lead Formed	SD1122BD
Description	200V, 10 ohms

SCHEMATIC DIAGRAM

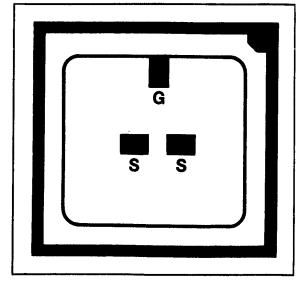


PACKAGE DIMENSIONS TO-92, LEAD FORMED



Lead-formed to TO-18 pin circle.
All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

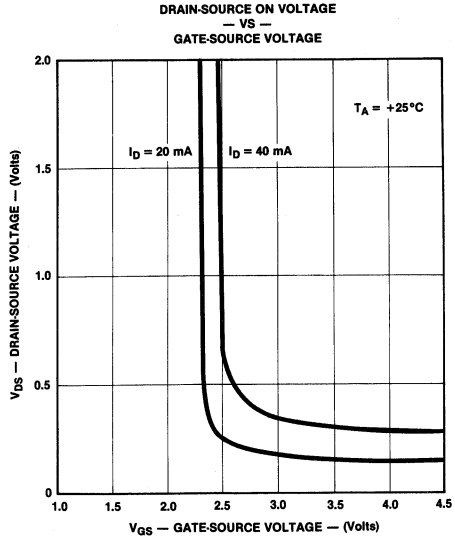
Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

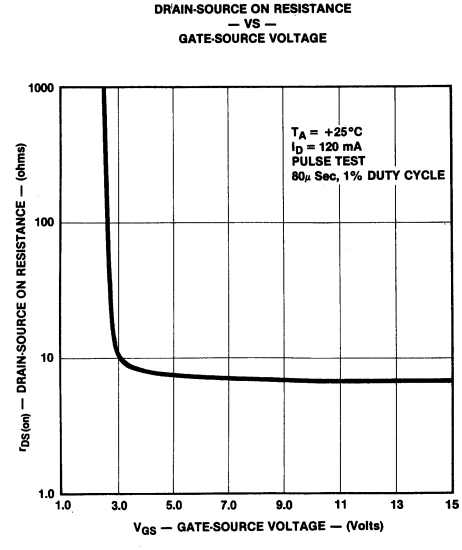
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1122 MIN	SD1122 TYP	SD1122 MAX	UNITS	TEST CONDITIONS
1	STATIC	B_{VDSS}	Drain Source Breakdown Voltage	200	270		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate Source Threshold Voltage	0.8	1.9	2.4	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{DSX}	Drain-Source OFF Leakage Current		0.1	1.0	μA	V_{DS} = 70V, V_{GS} = 0.2V
5	STATIC	I_{DSS}				30	nA	V_{DS} = 130V, V_{GS} = 0
6	STATIC	$I_{D(on)}$	ON Drain Current	0.5			A	V_{DS} = 25V, V_{GS} = 15V (Note 1)
7	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance		7.5	10	ohms	I_D = 120mA (Note 1), V_{GS} = 5.0V
8	STATIC				11	28		I_D = 20mA, V_{GS} = 2.6V
9	DYNAMIC	g_{fs}	Common-Source Forward Transcond.		300		mmhos	V_{DS} = 25V, I_D = 0.5A f = 1KHz (Note 1)
10	DYNAMIC	c_{iss}	Common-Source Input Capacitance		80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	c_{rss}	Common-Source Reverse Transfer Capacitance		1.3			
12	DYNAMIC	c_{oss}	Common-Source Output Capacitance		10.5			

Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS





TOPAZ SEMICONDUCTOR

SD1124

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS POWER FETs

FEATURES

- **Inherent Current Sharing Capability when Paralleled**
- **Simple Straight-Forward DC Biasing**
- **Extended Safe Operating Area**
- **Inherently Temperature Stable — Output Current Decreases as Temperature Increases**

APPLICATIONS

- **High-Speed Pulse Amplifiers**
- **Logic Buffers**
- **Line Drivers**
- **Analog Switches**
- **Motor Controls**
- **Power Supplies**

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage 60V
Drain-Gate Voltage (V_{GS} = 0) 60V
Gate-Source Voltage ..... ±30V
Continuous Device Dissipation (Note 2) 0.3W
Linear Derating Factor (Note 2) ..... 2.4mW/°C
Continuous Drain Current (Note 2) 0.2A
Peak Drain Current (Note 1, Note 2) 1.0A
Continuous Device Dissipation (Note 1, Note 2) 1.0W
Linear Derating Factor (Note 1, Note 2) ..... 8.0mW/°C
Thermal Resistance, Junction to case ..... 125°C/W
Operating Junction Temperature Range ..... −55 to +150°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (1/6″ from mounting surface for 30 Sec) ..... +260°C

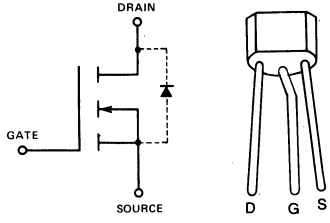
Note 1: T_{CASE} = +25°C

Note 2: Not applicable to chips. Final value depends upon mounting substrate.

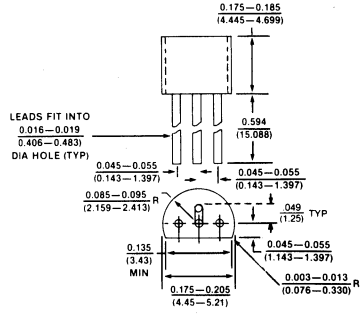
ORDERING INFORMATION

Sorted Chips in Carriers	SD1124CHP
TO-92 Pkg-Lead Formed	SD1124BD
Description	60V, 5 ohms

SCHEMATIC DIAGRAM

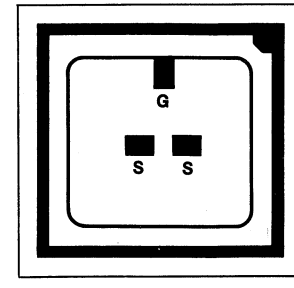


PACKAGE DIMENSIONS TO-92, LEAD FORMED



Lead-formed to TO-18 pin circle.
All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .054 x .056 x .013 inches
Drain is backside contact.

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

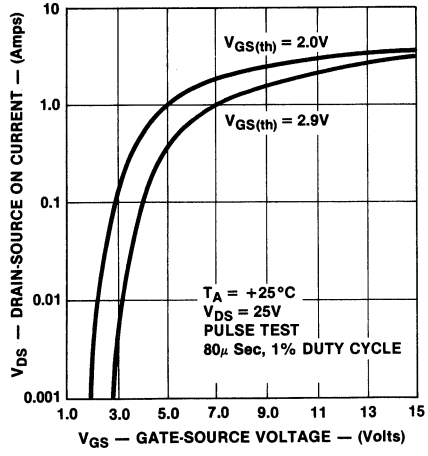
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD1124 MIN	SD1124 TYP	SD1124 MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain Source Breakdown Voltage	60	100		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate Source Threshold Voltage	0.8	2.1	3.0	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{DS}	Drain-Source OFF Leakage Current		0.1	1.0	μA	V_{DS} = 48V, V_{GS} = 0
5	STATIC	I_{DSS}	Drain-Source OFF Leakage Current			0.5	μA	V_{DS} = 25V, V_{GS} = 0
6	STATIC	$I_{D(on)}$	ON Drain Current	1.0			A	V_{DS} = 25V, V_{GS} = 15V (Note 1)
7	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance		2.8	5.0	ohms	I_D = 200mA, V_{GS} = 10V (Note 1)
8	DYNAMIC	g_{fs}	Common-Source Forward Transcond.		300		mmhos	V_{DS} = 25V, I_D = 0.2A f = 1KHz (Note 1)
9	DYNAMIC	c_{iss}	Common-Source Input Capacitance		80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
10	DYNAMIC	c_{rss}	Common-Source Reverse Transfer Capacitance		1.3		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	c_{oss}	Common-Source Output Capacitance		10.5		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	t_{on}	Turn ON Time		2.0	5.0	nSec	V_{DD} = 25V, $I_{D(on)}$ = 0.2A R_L = 23Ω, R_G = 51Ω
13	DYNAMIC	t_{off}	Turn OFF Time		2.0	5.0	nSec	V_{DD} = 25V, $I_{D(on)}$ = 0.2A R_L = 23Ω, R_G = 51Ω

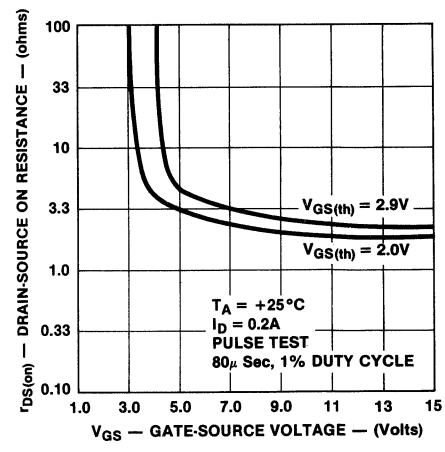
Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS

DRAIN-SOURCE ON CURRENT — VS — GATE-SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE — VS — GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

SD1127

N-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FET ULTRA LOW-LEAKAGE

FEATURES

- Drain-Source Leakage (I_{DSS}), 1.0nA max
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Switches
- Low-Leakage Solid State Relays
- High-Speed Pulse Amplifiers
- Logic Interfaces
- Line Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +60V
Drain-Gate Voltage (V_{GS} = 0) ..... +60V
Gate-Source Voltage ..... ±30V
Continuous Drain Current

	T_A = +25°C	T_C = +25°C
SD1127BD	.20A	.36A

Peak Pulsed Drain Current 2.0A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C
SD1127BD	0.30W	1.0W

Linear Derating Factor

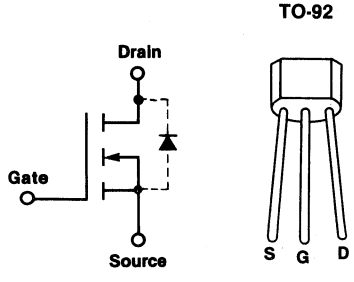
	T_A = +25°C	T_C = +25°C
SD1127BD	3.0mW/°C	10mW/°C

Operating Junction and Storage Temperature Range
-55°C to +150°C
Lead Temperature (1/16" from mounting surface for 30 sec.) ..... +260°C

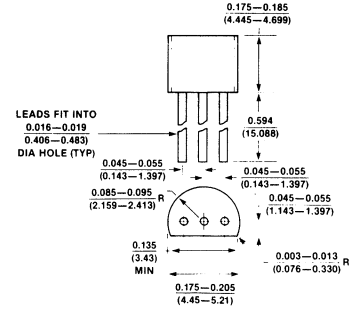
ORDERING INFORMATION

TO-92 Plastic Package	SD1127BD
Sorted Chips in Waffle Pack	SD1127CHP
Description	60 Volt, 4.0 ohm

PIN CONFIGURATION

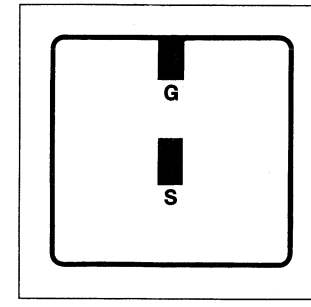


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .0445 x .0460 x .013 inches
Drain is backside contact.

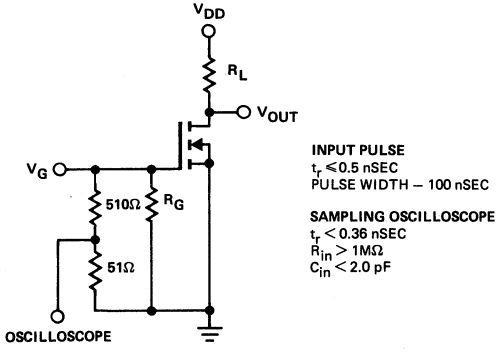
Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

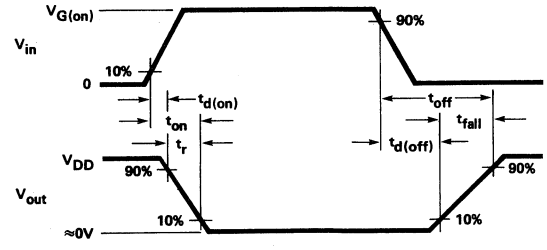
#		CHARACTERISTIC		SD1127 MIN	SD1127 TYP	SD1127 MAX	UNIT	TEST CONDITION
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60	90		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8		2.4	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC					10		T_A = +125°C
5	STATIC	I_{DSS}	Drain-Source OFF Leakage Current			1.0	nA	V_{DS} = 30V, V_{GS} = 0
6	STATIC					100		T_A = +125°C
7	STATIC	$I_{D(on)}$	ON Drain Current	2.0	3.5		A	V_{DS} = 25V, V_{GS} = 10V (Note 1)
8	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		3.2	5.0	ohms	V_{GS} = 5V, I_D = 0.3A (Note 1)
9	STATIC				2.9	4.0		V_{GS} = 10V, I_D = 1.0A (Note 1)
10	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	250	500		mmhos	V_{DS} = 25V, I_D = 1.0A f = 1KHz (Note 1)
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		80		pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		pF	
13	DYNAMIC	C_{oss}	Common-Source Output Capacitance		15		pF	
14	DYNAMIC	t_{on}	Turn-On Time		4.0	6.0	nSec	V_{DD} = 25V R_L = 25 ohms R_G = 51 ohms $V_{G(on)}$ = 10V
15	DYNAMIC	t_{off}	Turn-Off Time		4.0	6.0	nSec	

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT



TEST WAVEFORMS



TOPAZ SEMICONDUCTOR

SD1137, TN0106 TN0110

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-92 Plastic Package	SD1137BD	TN0106N3	TN0110N3
Sorted Chips in Carriers	SD1137CHP	TN0106ND	TN0110ND
Description	60V, 2.5 ohm	60V, 3.0 ohm	100V, 3.0 ohm

FEATURES

- Low Threshold,, $V_{GS(th)}$1.5V max
- Low Output and Transfer Capacitance
- Extended Safe Operating Area
- Complementary P-Channel Drivers Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Drain-Source Voltage
SD1137, TN0106 ..... +60V
TN0110 ..... +100V
SD1137, TN0106 ..... +60V
TN0110 ..... +100V
Gate-Source Voltage ..... ±30V
Continuous Drain Current

	T_A = +25°C	T_C = +25°C
SD1137BD	.25A	.46A
TN0106N3, TN0110N3	.23A	.42A

Peak Pulsed Drain Current ..... +2.0A
Continuous Device Dissipation

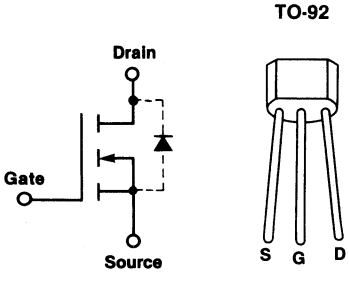
	T_A = +25°C	T_C = +25°C
TO-92 (N3 & BD) pkg	0.30W	1.0W

Linear Derating Factor

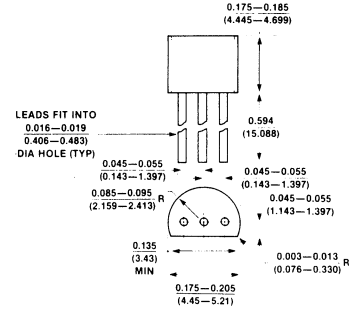
	T_A = +25°C	T_C = +25°C
TO-92 (N3 & BD) pkg	3.0mW/°C	10mW/°C

Operating Junction and Storage Temperature Range -55°C to +150°C
Lead Temperature (1/16" from mounting surface for 30 sec) ..... +250°C

PIN CONFIGURATION

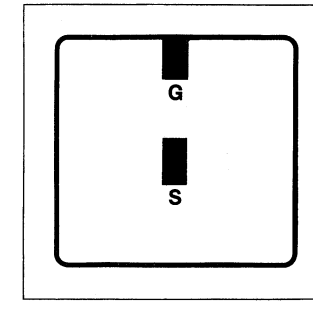


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .0445 x .0460 x .013 inches
Drain is backside contact.

TOPAZ SEMICONDUCTOR • 1971 N. Capitol Ave., San Jose, CA 95132-3799 • 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

#	PARAMETER	SD1137 MIN	SD1137 TYP	SD1137 MAX	TN0106 MIN	TN0106 TYP	TN0106 MAX	TN0110 MIN	TN0110 TYP	TN0110 MAX	UNIT	CONDITIONS		
1	BV_{DSS} Drain-Source Breakdown Voltage	60	90		60	90		100	115		V	I_D = 1.0mA, V_{GS} = 0		
2				100								V_{DS} = 48V	T_A = +125°C	
3							500					V_{DS} = 48V	V_{GS} = 0	
4	Drain-Source									500		V_{DS} = 80V		
5	I_{DSS} Off Leakage		.01	1.0								V_{DS} = 60V		
6	Current					.01	10				μA	V_{DS} = 60V	V_{GS} = 0	
7									.01	10		V_{DS} = 100V		
8	Gate-Body			±1.0			±1.0			±1.0	μA	V_{GB} = ±30V	V_{DS} = 0	
9	I_{GBS} Leakage Current			1.0			10			10	nA	V_{GB} = ±20V		
10	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5		1.5	0.5		1.5	0.5		1.5	V	V_{DS} = V_{GS}, I_D = 1.0mA		
11	$r_{DS(on)}$ Drain-Source			4.5			4.5			4.5	ohms	V_{GS} = 5V, I_D = .25A		(Note 1)
12	On Resistance			2.5								V_{GS} = 10V	I_D = 1.0A	
13							3.0			3.0			I_D = 0.5A	
14	$I_{D(on)}$ On Drain Current				.75			.75			A	V_{GS} = 5V	V_{DS} = 25V	
15		2.0			2.0			2.0				V_{GS} = 10V		
16	g_{fs} Common-Source	300	500								mmhos	V_{DS} = 25V	I_D = 0.5A	
17	Forward Transcond.				225	500		225	500			V_{DS} = 20V	f = 1KHz	
18	V_{SD} Source-Drain			1.5							V	I_{SD} = 0.8A	V_{GS} = 0	
19	Forward Voltage						1.5			1.5		I_{SD} = 0.5A		
20	c_{iss} Common-Source Input Capacitance			60			60			60	pF	V_{DS} = 25V V_{GS} = 0 f = 1MHz		
21	c_{oss} Common-Source Output Capacitance		11	35		11	35		11	35				
22	c_{rss} Common-Source Reverse Transfer Capacitance		1.5	8.0		1.5	8.0		1.5	8.0				
23	t_{on} Turn ON Time		8.0	10		8.0	10		8.0	10	nS	V_{DD} = 25V, $V_{G(on)}$ = 10V		
24	t_{off} Turn OFF Time		8.0	12		8.0	12		8.0	12		R_G = 51Ω, R_L = 25Ω		

NOTE 1: Pulse Test, 80μSec, 1% Duty Cycle

TOPAZ SEMICONDUCTOR

SD1200, SD1201

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS FETs

FEATURES

- **Extended Safe Operating Area**
- **Simple, Straight-Forward, DC Biasing**
- **Low Capacitance, C_{oss} 1.5 pF (typ.)**

APPLICATIONS

- **Display Drivers**
- **Reed Relays**
- **Low-Power, High-Voltage Drivers**

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

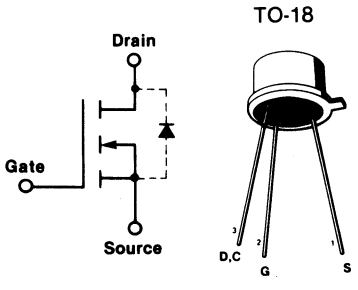
Drain-Source Voltage
SD1200 ..... 450V
SD1201 ..... 400V
Drain-Gate Voltage (V_{GS} = 0)
SD1200 ..... 450V
SD1201 ..... 400V
Gate-Source Voltage ..... ±30V
Continuous Drain Current
SD1200DD, SD1201DD 20mA
Peak Drain Current
SD1200DD, SD1201DD 40mA

Continuous Device Dissipation
SD1200DD, SD1201DD 300mW
Linear Derating Factor
SD1200DD, SD1201DD ..... 2.4mW/°C
Operating Junction Temperature
Range ..... −55 to +150°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (1/16″ from
mounting surface for 30 Sec) ..... +260°C

ORDERING INFORMATION

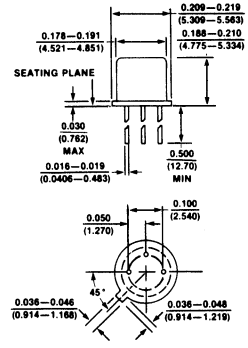
Sorted Chips in Carriers	SD1200CHP	SD1201CHP
TO-18 Package	SD1200DD	SD1201DD
Description	450V, 700 ohm	400V, 500 ohm

SCHEMATIC DIAGRAM



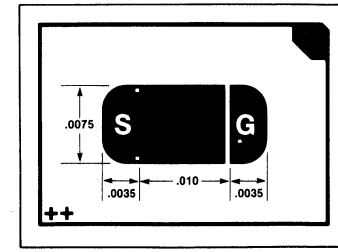
Drain common to case.

PACKAGE DIMENSIONS TO-18



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Drain is backside contact.
Dimensions: .025 x .034 x .013 inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

#		CHARACTERISTIC	SD1200 MIN	SD1200 TYP	SD1200 MAX	SD1201 MIN	SD1201 TYP	SD1201 MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	450	500		400	450		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage	1.0	4.0	5.0	1.0	4.0	5.0	V	I_D = 10μA, V_{DS} = V_{GS}
3	STATIC	I_{GBS} Gate-Body Leakage Current		.02	1.0		.02	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{DSS} Drain-Source OFF Leakage Current		1.0	100				nA	V_{DS} = 360V, V_{GS} = 0
5	STATIC	I_{DSS} Drain-Source OFF Leakage Current					1.0	100	nA	V_{DS} = 320V, V_{GS} = 0
6	STATIC	$I_{D(on)}$ ON Drain Current	20			20			mA	V_{DS} = 25V, V_{GS} = 15V
7	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		400	700		300	500	ohms	I_D = 1mA, V_{GS} = 15V
8	DYNAMIC	g_{fs} Common-Source Forward Transconductance		10			10		mmhos	V_{DS} = 20V, I_D = 20mA f = 1KHz
9	DYNAMIC	C_{iss} Common-Source Input Capacitance		8.0			8.0		pF	V_{DS} = 20V, V_{GS} = 0 f = 1MHz
10	DYNAMIC	C_{rss} Common-Source Reverse Transfer Capacitance		0.8			0.8		pF	V_{DS} = 20V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	C_{oss} Common-Source Output Capacitance		1.5			1.5		pF	V_{DS} = 20V, V_{GS} = 0 f = 1MHz

TOPAZ SEMICONDUCTOR

SD1202

N-CHANNEL ENHANCEMENT-MODE HIGH-VOLTAGE D-MOS FETs

FEATURES

- Extended Safe Operating Area
- Simple, Straight-Forward, DC Biasing
- Low Capacitance (C_{OSS} 1.5 pF typ.)
- Low Leakage (I_{DSS} 1.0 nA typ. @ 180V)
- High Gate Breakdown (±100V min.)

APPLICATIONS

- Display Drivers
- AC-DC Relays
- Reed Relays
- Low-Power, High-Voltage Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

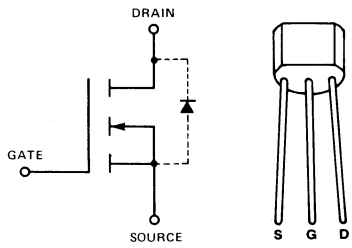
Drain-Source Voltage	200V
Drain-Gate Voltage (V_{GS} = 0)	200V
Gate-Source Voltage	±100V
Continuous Drain Current (Note 1)	20mA
Peak Drain Current (Note 1)	40mA
Continuous Device Dissipation (Note 1)	300mW
Linear Derating Factor (Note 1)	2.4mW/°C
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/6″ from mounting surface for 30 Sec)	+260°C

Note 1: Not applicable to chips. Final value depends upon mounting substrate.

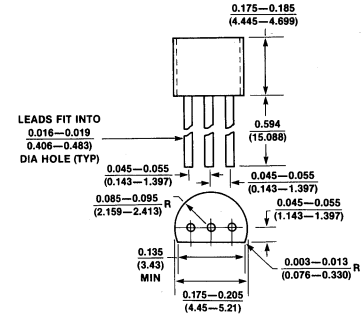
ORDERING INFORMATION

Sorted Chips in Carriers	SD1202CHP
TO-92 Package	SD1202BD
Description	200V, 250 ohm

SCHEMATIC DIAGRAM

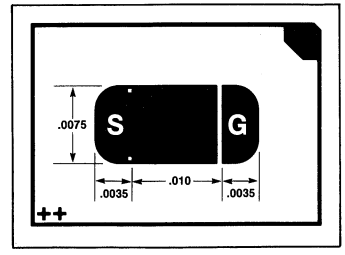


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Drain is backside contact.
Dimensions: .025 x .034 x .013 inches

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

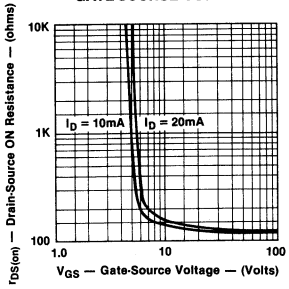
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

#		CHARACTERISTIC		SD1202 MIN	SD1202 TYP	SD1202 MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain Source Breakdown Voltage	200	260		V	I_D = 1.0μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate Source Threshold Voltage	1.0		5.0	V	I_D = 10μA, V_{DS} = V_{GS}
3	STATIC	I_{GBS}	Gate-Body Leakage Current		.02	1.0	nA	V_{GS} = 100V, V_{DS} = 0
4	STATIC	I_{DSS}	Drain-Source OFF Leakage Current		1.0	3.0	nA	V_{DS} = 180V, V_{GS} = 0
5	STATIC	$I_{D(on)}$	Drain Source ON Current	40	55		mA	V_{DS} = 25V, V_{GS} = 10V
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		150	250	ohms	I_D = 10mA, V_{GS} = 10V
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance		13		mmhos	V_{DS} = 20V, I_D = 20mA f = 1KHz (Note 1)
8	DYNAMIC	c_{iss}	Common-Source Input Capacitance		8.0		pF	V_{DS} = 20V, V_{GS} = 0 f = 1MHz
9	DYNAMIC	c_{rss}	Common-Source Reverse Transfer Capacitance		0.8		pF	
10	DYNAMIC	c_{oss}	Common-Source Output Capacitance		1.5		pF	

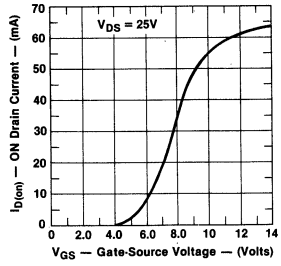
Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unelss otherwise noted.)

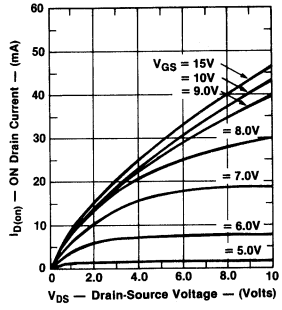
DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



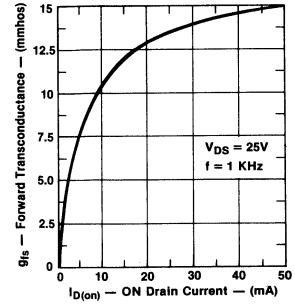
TRANSFER CHARACTERISTIC



SATURATION CHARACTERISTIC



FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD1500, SD1501

N-CHANNEL ENHANCEMENT-MODE VERTICAL D-MOS FET

FEATURES

- Guaranteed BV_{DSS} of 600V min
- Low Output and Transfer Capacitance
- Extended Safe Operating Area
- Available in Low Cost TO-92 Package

APPLICATIONS

- Outpulser Switching
- High Speed Pulse Amplifiers
- Solid-State Relays
- Display Drivers
- High Voltage ATE
- Telecommunications Switching

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage
- SD1500 ..... 600V
- SD1501 ..... 550V

Drain-Gate Voltage (V_{GS} = 0)
- SD1500 ..... 600V
- SD1501 ..... 550V

Gate-Source Voltage ..... ±30V

Continuous Drain Current

	T_A = +25°C	T_C = +25°C	
SD1500BD, SD1501BD	50	100	mA

Peak Pulsed Drain Current 200mA

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C
SD1500BD, SD1501BD	300mW	1.0W

Linear Derating Factor

	T_A = +25°C	T_C = +25°C	
SD1500BD, SD1501BD	3.0	1.0	mW/°C

Operating Junction Temperature Range ..... -55 to +125°C

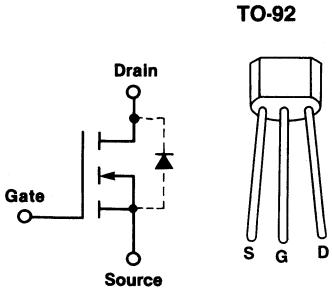
Storage Temperature Range ..... -55 to +125°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

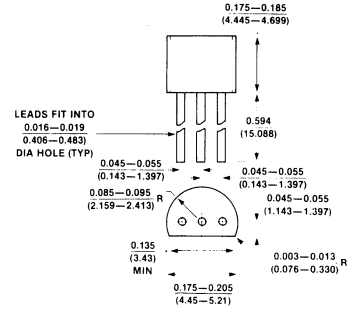
ORDERING INFORMATION

TO-92 Plastic Package	SD1500BD	SD1501BD
Sorted Chips in Waffle Pack	SD1500CHP	SD1501CHP
Description	600 Volt, 60 ohm	550 Volt, 60 ohm

CONFIGURATION

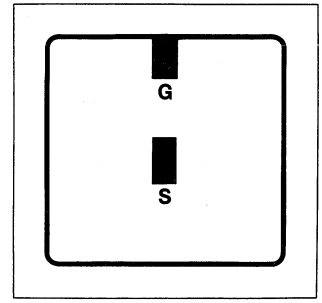


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



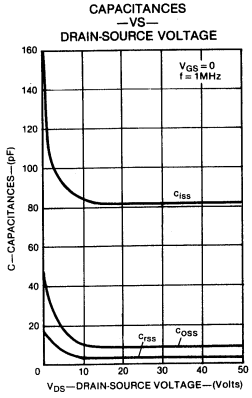
Dimensions: .055 x .057 x .013 inches
Drain is backside contact.

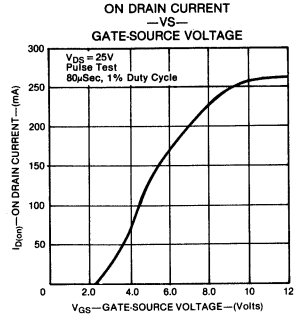
Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

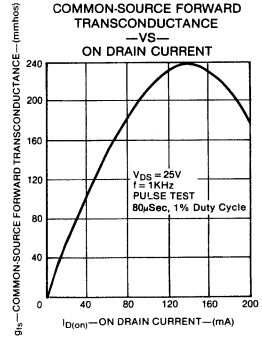
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

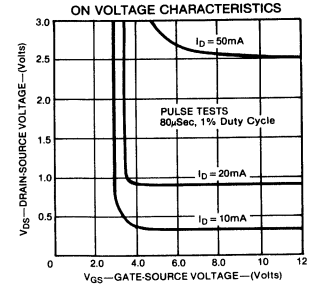
#		CHARACTERISTIC	SD1500 MIN	SD1500 TYP	SD1500 MAX	SD1501 MIN	SD1501 TYP	SD1501 MAX	UNIT	TEST CONDITION
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	600	700		550	600		V	I_D = 10μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage	1.0	2.9	4.0	1.0	2.9	4.0	V	V_{DS} = V_{GS}, I_D = 1mA
3	STATIC	I_{GBS} Gate-Body Leakage Current		.03	1.0		.03	1.0	nA	V_{GS} = 20V, V_{DS} = 0
4	STATIC	I_{GBS} Gate-Body Leakage Current			10			10	nA	V_{GS} = 20V, V_{DS} = 0, T_A = +125°C
5	STATIC	I_{DSS} Drain-Source OFF Leakage Current		0.1	1.0				μA	V_{DS} = 480V, V_{GS} = 0
6	STATIC	I_{DSS} Drain-Source OFF Leakage Current			50				μA	V_{DS} = 480V, V_{GS} = 0, T_A = +125°C
7	STATIC	I_{DSS} Drain-Source OFF Leakage Current					0.1	1.0	μA	V_{DS} = 440V, V_{GS} = 0
8	STATIC	I_{DSS} Drain-Source OFF Leakage Current						50	μA	V_{DS} = 440V, V_{GS} = 0, T_A = +125°C
9	STATIC	$I_{D(on)}$ ON Drain Current	100	260		100	260		mA	V_{DS} = 25V, V_{GS} = 15V (Note 1)
10	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		45	60		45	60	ohms	V_{GS} = 15V, I_D = 20mA
11	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance								(Note 1)
12	DYNAMIC	g_{fs} Common-Source Forward Transcond.	100	215		100	215		mmhos	V_{DS} = 25V, I_D = 100mA, f = 1KHz (Note 1)
13	DYNAMIC	C_{iss} Common-Source Input Capacitance		80	100		80	100	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz
14	DYNAMIC	C_{rss} Common-Source Reverse Transfer Capacitance		1.0	2.0		1.0	2.0	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz
15	DYNAMIC	C_{oss} Common-Source Output Capacitance		6.0	10		6.0	10	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz
16	DYNAMIC	t_{on} Turn-On Time		7.0	12		7.0	12	nSec	V_{DD} = 25V, R_L = 51 ohms, R_G = 51 ohms, $V_{G(on)}$ = 10V
17	DYNAMIC	t_{off} Turn-Off Time		7.0	12		7.0	12	nSec	V_{DD} = 25V, R_L = 51 ohms, R_G = 51 ohms, $V_{G(on)}$ = 10V

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise noted)









TOPAZ SEMICONDUCTOR

SD2100

N-CHANNEL DEPLETION-MODE D-MOS FET

FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Pin and Function Compatible to Industry Standard J-FETs with addition of Substrate Bias Pin.

APPLICATIONS

- High-Speed Analog Switches
- Wide-Band RF Amplifiers
- Cascode Amplifiers

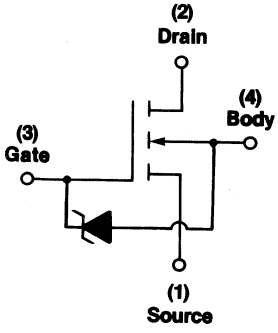
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage	+20V
V_{SD} Source-Drain Voltage	+10V
V_{DB} Drain-Body Voltage	+25V
V_{SB} Source-Body Voltage	+15V
V_{GD} Gate-Drain Voltage	+25V
V_{GS} Gate-Source Voltage	+25V
V_{GB} Gate-Body Voltage	+25V
I_D Continuous Drain Current	+50 mA
P_D Total Device Dissipation	360 mW
Derating Factor	2.88 mW/°C
T_j Operating Junction Temperature Range	-55 to +150°C
T_S Storage Temperature Range	-55 to +150°C
T_L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260°C

ORDERING INFORMATION

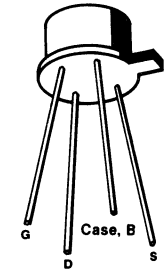
TO-72 Hermetic Package	SD2100DE
with Shorting Ring on leads	SD2100DE/R
Description	20V, 150Ω

SCHEMATIC DIAGRAM

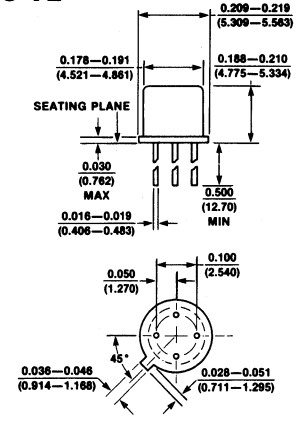


Body internally connected to Case.

PIN CONFIGURATION



PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20			V	I_D = 10nA, V_{GS} = V_{BS} = –5V	
2		BV_{SD}	Source-Drain Breakdown Voltage	10				I_S = 10nA, V_{GD} = V_{BD} = –5V	
3		BV_{DB}	Drain-Body Breakdown Voltage	25				I_D = 10nA, V_{GB} = 0 Source Open	
4		BV_{SB}	Source-Body Breakdown Voltage	15				I_S = 10μA, V_{GB} = 0 Drain open	
5		$I_{GSS(fwd)}$	Forward Gate Leakage Current			1.0	nA	V_{GS} = 25V, V_{DS} = V_{BS} = 0	
6		I_G	Gate Operating Current		–3.0	–100	pA	V_{DG} = 20V, I_D = 5.0 mA, V_{BS} = –5.6V	
7					–0.7	–10	nA		T_A = +125°C
8		$V_{GS\ (off)}$	Gate-Source Cutoff Voltage	–1.0		–5.0	V	V_{DS} = 10V, I_D = 1.0μA, V_{BS} = –5.6V	
9		$V_{GS(on)}$	Gate-Source ON Voltage	–0.3		–3.0		V_{DG} = 10V, I_D = 5mA, V_{BS} = –5.6V	
10		I_{DSX}	Zero Gate Voltage[1] Drain Current	7.0		40	mA	V_{DS} = 10V, V_{GS} = 0, V_{BS} = –5.6V	
11				5.0					T_A = +125°C
12		$r_{DS(ON)}$	Drain-Source ON Resistance		100	150	ohms	I_D = 1.0mA, V_{GS} = 0, V_{BS} = –5.6V	
13	DYNAMIC	g_{fs}	Common-Source[1] Forward Transconductance	5.0	7.5	10	mmhos	V_{DG} = 10V, I_D = 5.0 mA, V_{BS} = –5.6V	f = 1 KHz
14		g_{os}	Common-Source Output Conductance		200	300	μmhos		
15		C_{iss}	Common-Source Input Capacitance		3.5		pF		f = 1 MHz
16		C_{oss}	Common-Source Output Capacitance		1.2				
17		C_{rss}	Common-Source Reverse Transfer Capacitance		0.3				
18		$C_{(gs\ +\ sb)}$	Source Node Capacitance		4.5				

Note 1: Pulse Test, 80μsec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS: See TZ5911

TOPAZ SEMICONDUCTOR

SD2107

P-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- Gate Stand-off Voltage, ±40V min.
- Low Output and Transfer Capacitances
- Wide Variety of Packages
- N-Channel Complements Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Pulse Amplifiers
- Motor Controls
- Logic Interfaces

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD2107CHP
TO-18 Hermetic Package	SD2107DD
TO-39 Hermetic Package	SD2107HD
TO-92 Plastic Package	SD2107BD
TO-237 (92^{+}) Plastic Package	SD2107AD
Description	-100V, 5.0 ohm

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... -100V

Drain-Gate Voltage (V_{GS}= 0) ..... -100V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_A = 25°C	T_C = 25°C
SD2107AD	-.26A	-.43A
SD2107BD	-.24A	-.32A
SD2107DD	-.26A	-.43A
SD2107HD	-.44A	-.81A

Peak Pulsed Drain Current ..... -1.1A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C	
SD2107AD	0.36	1.8	W
SD2107BD	0.3	1.0	W
SD2107DD	0.36	1.8	W
SD2107HD	1.0	6.25	W

Linear Derating Factor

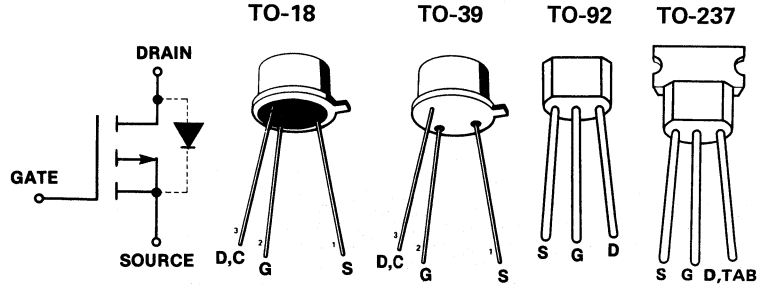
	T_A = +25°C	T_C = +25°C	
SD2107AD	2.88	14.4	mW/°C
SD2107BD	2.4	8.0	mW/°C
SD2107DD	2.88	14.4	mW/°C
SD2107HD	8.0	50	mW/°C

Operating Junction Temperature Range ..... -55 to +150°C

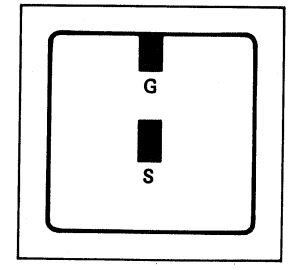
Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

PIN CONFIGURATIONS



CHIP CONFIGURATION



Dimensions: 0.0445 x 0.0460 x 0.013 inches
Drain is backside contact.

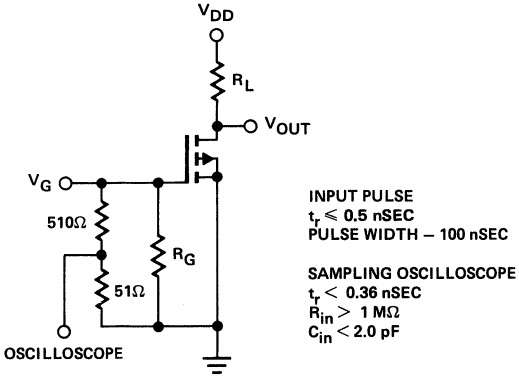
Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

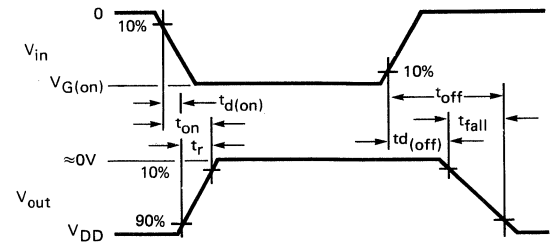
#		CHARACTERISTIC		SD2107 MIN	SD2107 TYP	SD2107 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-100	-120		V	I_D=-10μA	V_{GS} = 0
2				-100	-120			I_D=-1.0mA	
3		I_{DSS}	Drain-Source OFF Leakage Current			-100	nA	V_{DS} = -80V	
4						-5.0	μA	V_{GS} = 0	T_A=+125°C
5		I_{GBS}	Gate-Body Leakage Current			±10	nA	V_{GS} = ±30V	
6						±1.0	μA	V_{GS}= ±40V	V_{DS} = 0
7		$V_{GS(th)}$	Gate-Source Threshold Voltage	-1.5		-3.5	V	V_{DS} = V_{GS}, I_D = -1.0mA	
8		$r_{DS(on)}$	Drain-Source (1) ON Resistance			15	ohms	V_{GS} = -5V, I_D = -0.1A	
9					3.9	5.0		V_{GS} = -10V,	
10						8.0		I_D = -0.5A	T_A=+125°C
11		$I_{D(on)}$	ON Drain Current (1)	-1.1			A	V_{DS} = -25V, V_{GS} = -10V	
12	DYNAMIC	g_{fs}	Common-Source (1) Forward Transcond.	200	260		mmhos	V_{DS} = -25V, I_D = -0.5A f = 1KHz	
13		C_{iss}	Common-Source Input Capacitance		60	80	pF	V_{DS} = -25V, V_{GS} = 0 f = 1MHz	
14		C_{rss}	Common-Source Reverse Transfer Capacitance		5.0	8.0			
15		C_{oss}	Common-Source Output Capacitance		10.5	20			
16		t_{on}	Turn-On Time			16	nSec	V_{DD} = -25V R_L = 51 ohms R_G = 51 ohms $V_{G(on)}$= -10V	
17		t_{off}	Turn-Off Time			16			

Note 1: Pulse Test, 80μ Sec, 1% Duty Cycle

SWITCHING TIME TEST CIRCUIT

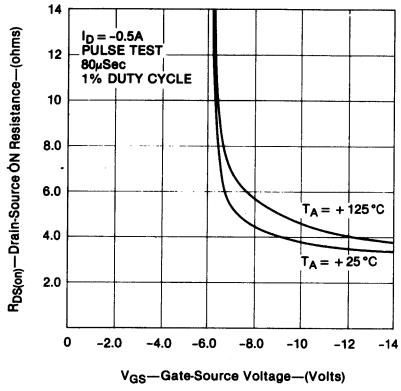


TEST WAVEFORMS

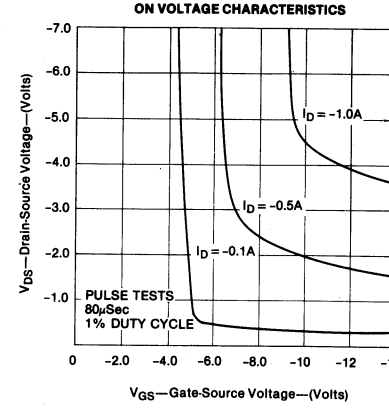


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

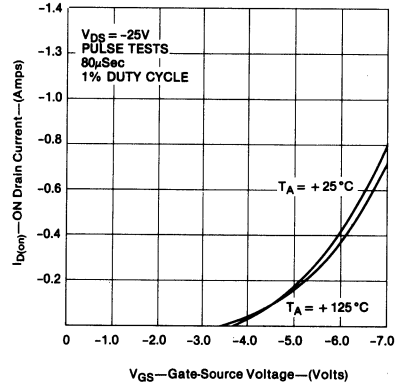
DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



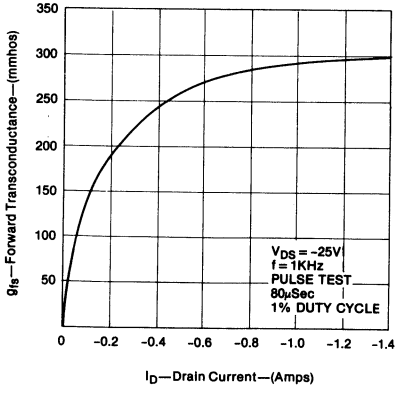
ON VOLTAGE CHARACTERISTICS



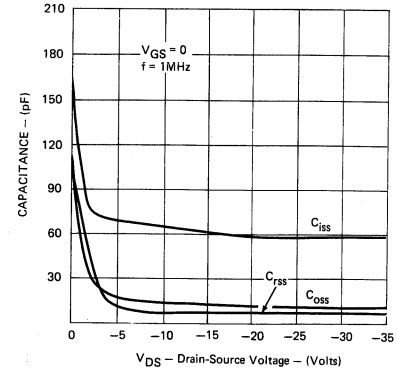
ON DRAIN CURRENT —VS— GATE SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



CAPACITANCES —VS— DRAIN-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

SD2200

N-CHANNEL DEPLETION-MODE D-MOS FET

FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Pin and Function Compatible to Industry Standard J-FETs with addition of Substrate Bias Pin

APPLICATIONS

- High-Speed Analog Switches
- Wide-Band RF Amplifiers
- Cascode Amplifiers

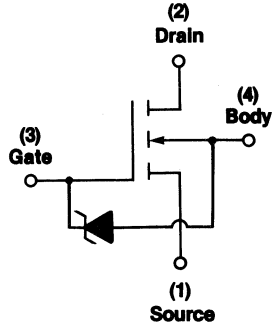
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage	+20V
V_{SD} Source-Drain Voltage	+10V
V_{DB} Drain-Body Voltage	+25V
V_{SB} Source-Body Voltage	+15V
V_{GD} Gate-Drain Voltage	+25V
V_{GS} Gate-Source Voltage	+25V
V_{GB} Gate-Body Voltage	+25V
I_D Continuous Drain Current	+100 mA
P_D Total Device Dissipation	360 mW
Derating Factor	2.88 mW/°C
T_j Operating Junction Temperature Range	-55 to +150°C
T_S Storage Temperature Range	-55 to +150°C
T_L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260°C

ORDERING INFORMATION

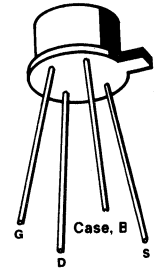
TO-72 Hermetic Package	SD2200DE
with Shorting Ring on leads	SD2200DE/R
Description	20V, 75Ω

SCHEMATIC DIAGRAM

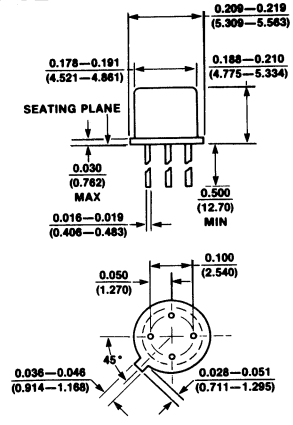


Body internally connected to Case

PIN CONFIGURATION



PACKAGE DIMENSIONS TO-72



All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

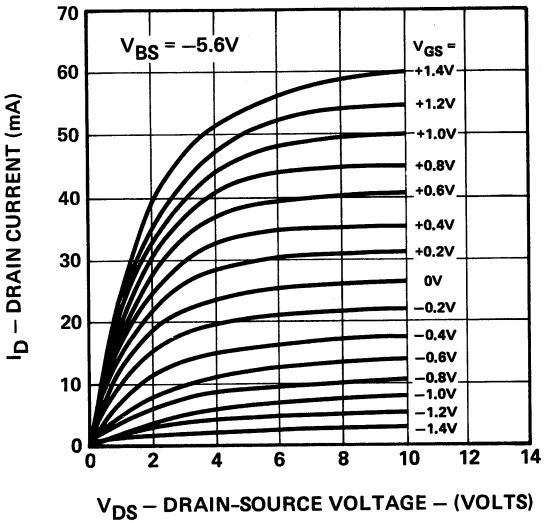
ELECTRICAL CHARACTERISTICS (T_A = +25°C, per side, unless otherwise noted)

#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20			V	I_D = 20nA, V_{GS} = V_{BS} = -5V	
2		BV_{SD}	Source-Drain Breakdown Voltage	10				I_S = 20nA, V_{GD} = V_{BD} = -5V	
3		BV_{DB}	Drain-Body Breakdown Voltage	25				I_D = 20nA, V_{GB} = 0 Source Open	
4		BV_{SB}	Source-Body Breakdown Voltage	15				I_S = 10μA, V_{GB} = 0 Drain open	
5		$I_{GSS(fwd)}$	Forward Gate Leakage Current			2.0	nA	V_{GS} = 25V, V_{DS} = V_{BS} = 0	
6		I_G	Gate Operating Current		-6.0	-100	pA	V_{DG} = 20V, I_D = 5.0 mA, V_{BS} = -5.6V	
7					-1.4	-10	nA	V_{BS} = -5.6V	T_A = +125°C
8		$V_{GS\ (off)}$	Gate-Source Cutoff Voltage	-1.0		-5.0	V	V_{DS} = 10V, I_D = 2.0μA, V_{BS} = -5.6V	
9		$V_{GS(on)}$	Gate-Source[1] ON Voltage	-0.3		-3.0		V_{DG} = 10V, I_D = 10mA, V_{BS} = -5.6V	
10		I_{DSX}	Zero Gate Voltage[1] Drain Current	14		60	mA	V_{DS} = 10V, V_{GS} = 0, V_{BS} = -5.6V	
11				10					T_A = +125°C
12		$r_{DS(ON)}$	Drain-Source ON Resistance		50	75	ohms	I_D = 1.0mA, V_{GS} = 0, V_{BS} = -5.6V	
13	DYNAMIC	g_{fs}	Common-Source[1] Forward Transconductance	10	15	20	mmhos	V_{DG} = 10V, I_D = 10 mA, V_{BS} = -5.6V	f = 1 KHz
14		g_{os}	Common-Source Output Conductance		380	600	μmhos		
15		C_{iss}	Common-Source Input Capacitance		7.0		pF		f = 1 MHz
16		C_{oss}	Common-Source Output Capacitance		2.4				
17		C_{rss}	Common-Source Reverse Transfer Capacitance		0.6				
18		$C_{(gs\ +\ sb)}$	Source Node Capacitance		9.0				

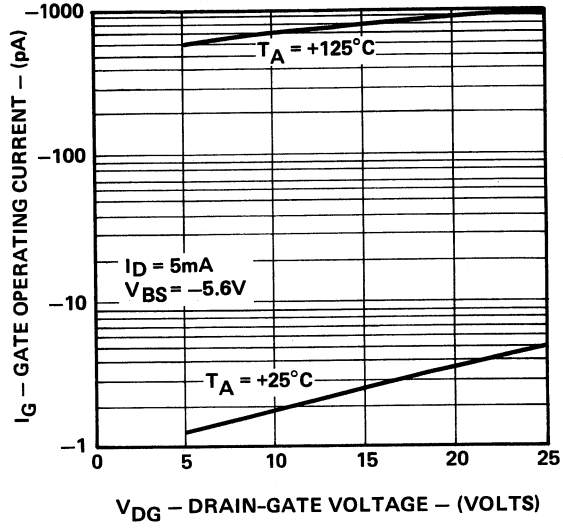
Note 1: Pulse Test, 80μsec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

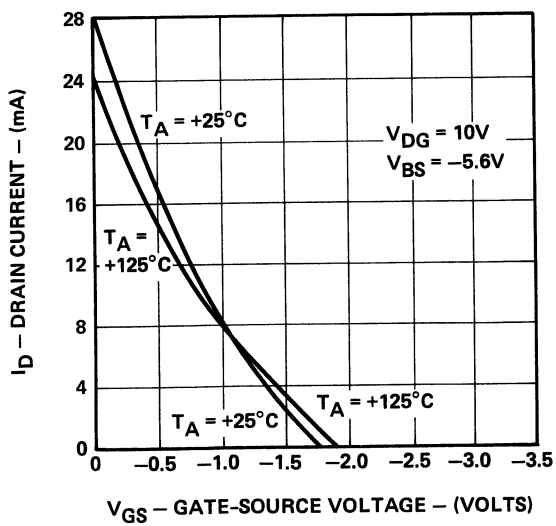
OUTPUT CHARACTERISTIC



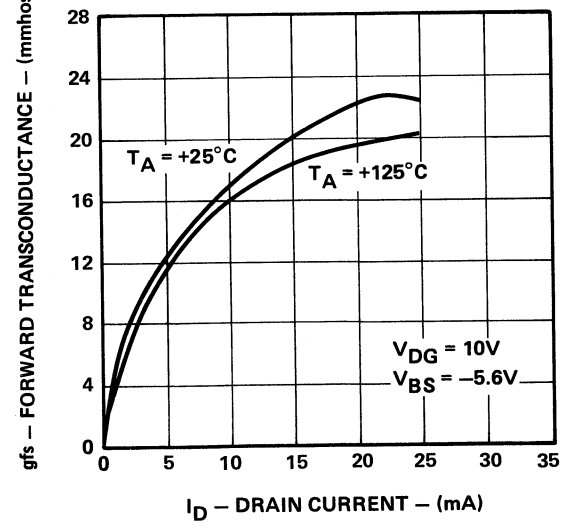
GATE OPERATING CURRENT —VS— DRAIN-GATE VOLTAGE



TRANSFER CHARACTERISTIC



FORWARD TRANSCONDUCTANCE —VS— DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD2204

P-CHANNEL ENHANCEMENT MODE D-MOS FET

ORDERING INFORMATION

TO-92 Plastic Package	SD2204BD
Description	-400V, 700Ω

FEATURES

- Ultra-Low Channel OFF Leakage, <-500pA
- Low Interelectrode Capacitances
- N-Channel Complements available, SD1201
- Gate Standoff Voltage, ±40V min.

APPLICATIONS

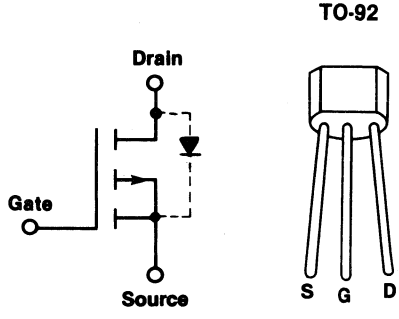
- High-Voltage Drivers
- High-Voltage Level Translators
- Reed Relay Replacements

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

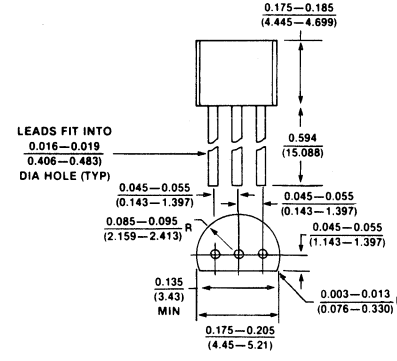
Drain-Source Voltage	-400V
Drain-Gate Voltage (V_{GS} = 0)	-400V
Gate-Source Voltage	±40V
Operating and Storage Temperature Range	-55 to +125°C
Lead Temperature (1/16" from mounting Surface for 10 sec.)	+260°C

	T_A = +25°C	T_C = +25°C
Continuous Drain Current	-15mA	-25mA
Continuous Device Dissipation	0.30W	1.0W
Linear Derating Factor	3.0mW/°C	10mW/°C

PIN CONFIGURATION



PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

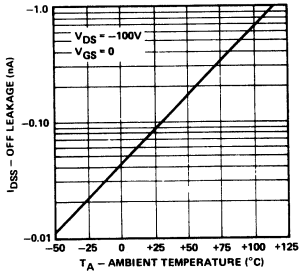
Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C per channel, unless otherwise noted)

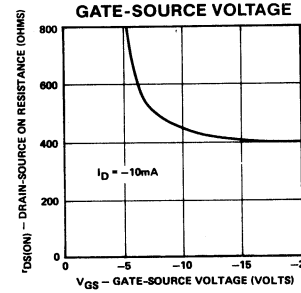
#		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain-Source	-400			V	I_D=-100μA, V_{GS} = 0
2			Breakdown Voltage	-400				I_D=-1.0μA
3		I_{DSS}	Drain-Source OFF Leakage Current			-500	pA	V_{DS} = -100V, V_{GS} = 0
4		I_{GBS}	Gate-Body			±1.0	nA	V_{GB} = ±20V, V_{DS} = 0
5			Leakage Current			±1.0	μA	V_{GB} = ±40V, V_{DS} = 0
6		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2.0		-5.0	V	V_{DS} = V_{GS}, I_D = -0.5mA
7		$r_{DS(on)}$	Drain-Source ON Resistance			700	ohms	I_D = -10mA, V_{GS} = -10V
8		$I_{D(on)}$	Drain-Source ON Current	-15			mA	V_{DS} = -25V, V_{GS} = -10V
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3.0			mmhos	V_{DS} = -25V, I_D = -5mA f = 1KHz
10		C_{iss}	Common-Source Input Capacitance		8.0	10	pF	V_{DS} = -25V, V_{GS} = 0, f = 1MHz
11		C_{OSS}	Common-Source Output Capacitance		1.5	2.0		
12			Common-Source Reverse Transfer Capacitance		0.8	1.0		
13		$t_{d(on)}$	Turn-ON Delay Time		6		nS	V_{DD} = -25V, $V_{G(on)}$ = -10V R_L = 500Ω R_G = 51Ω
14		t_r	Rise time		6			
15		$t_{d(off)}$	Turn-OFF Delay Time		8			
16		t_f	Fall Time		6			

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

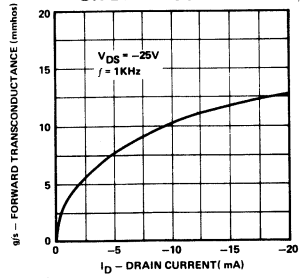
DRAIN-SOURCE OFF LEAKAGE —vs— AMBIENT TEMPERATURE



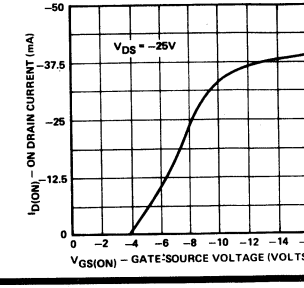
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

SD3300, SD3301

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD3300CHP	SD3301CHP
TO-39 (TO-205 AF) Hermtic Package	SD3300HD	SD3301HD
TO-92 Plastic Package	SD3300BD	SD3301BD
TO-237 (TO-92+) Plastic Package	SD3300AD	SD3301AD
Description	100V, 0.6 ohm	60V, 0.4 ohm

FEATURES

- Gate Stand-off Voltage, ±40V min.
- Continuous I_D of 1 Amp in small package
- Wide Variety of Packages

APPLICATIONS

- Motor Controls
- Line Drivers
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Drain-Source Voltage
- SD3300 ..... 100V
- SD3301 ..... 60V

Drain-Gate Voltage (R_{GS} = 1MΩ)
- SD3300 ..... 100V
- SD3301 ..... 60V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_C = +100°C	T_C = +25°C
SD3300AD	1.2A	1.9A
SD3300BD	1.0A	1.6A
SD3300HD	2.25A	3.5A
SD3301AD	1.4A	2.3A
SD3301BD	1.2A	1.9A
SD3301HD	2.7A	4.3A

Peak Pulsed Drain Current 8.0A

Maximum Power Dissipation

	T_C = +100°C	T_C = +25°C
HD, TO-39 Pkg.	6.0W	15W
BD, TO-92 Pkg.	1.2W	3.0W
AD, TO-237 Pkg.	1.7W	4.3W

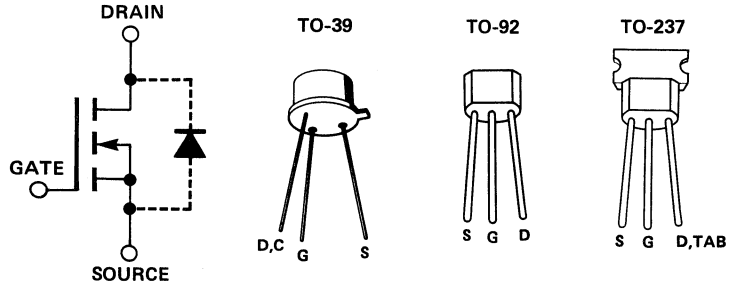
Linear Derating Factor

	Junction to Ambient (mW/°C)	Junction to Case (mW/°C)
HD, TO-39 Pkg.	8.0	120
BD, TO-92 Pkg.	3.2	24
AD, TO-237 Pkg.	4.8	34.4

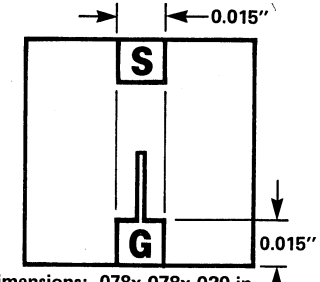
Operating Junction and Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

PIN CONFIGURATIONS



CHIP CONFIGURATION



Dimensions: .078x.078x.020 in.
Drain is backside contact.

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

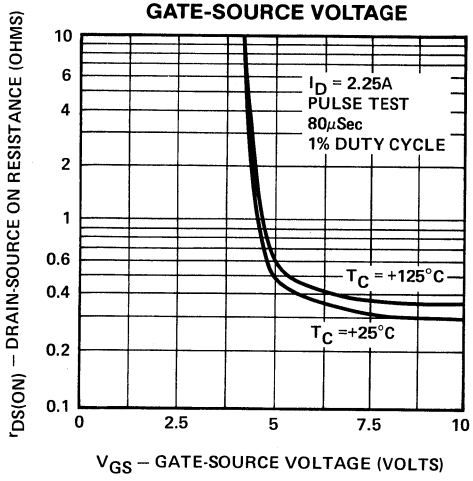
ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

#		CHARACTERISTIC	SD3300 MIN	SD3300 TYP	SD3300 MAX	SD3301 MIN	SD3301 TYP	SD3301 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	100	125		60	90		V	I_D = 250μA, V_{GS} = 0	
2		$V_{GS(th)}$ Gate-Source Threshold Voltage	1.0		3.0	1.0		3.0	V	V_{DS} = V_{GS}	
3			0.4			0.4				I_D = 250μA	T_C = +125°C
4		I_{GBS} Gate-Body Leakage Current			100			100	nA	V_{GS} = 20V, V_{DS} = 0	
5					200			200			T_C = +125°C
6					-100			-100		V_{GS} = -20V, V_{DS} = 0	
7		I_{DSS} Drain-Source OFF Leakage Current			1.0				μA	V_{DS} = 80V, V_{GS} = 0	
8					1000						T_C = +125°C
9								1.0		V_{DS} = 48V, V_{GS} = 0	
10								1000			T_C = +125°C
11		$I_{D(on)}$ ON Drain Current(1)	3.0			3.5			A	V_{DS} = 10V, V_{GS} = 10V	
12		$V_{DS(on)}$ Drain-Source(1) ON Voltage			1.8				V	V_{GS} = 10V, I_D = 3.0A	
13								1.4		V_{GS} = 10V, I_D = 3.5A	
14		$r_{DS(on)}$ Drain-Source(1) ON Resistance			0.6			0.4	ohms	V_{GS} = 10V	
15					1.08			0.72		I_D = 2.25A	T_C = +125°C
16	DYNAMIC	g_{fs} Common-Source(1) Forward Transcond.	1.0		3.0	1.0		3.0	S(℧)	V_{DS} = 10V, I_D = 2.25A	f = 1KHz
17		C_{iss} Common-Source Input Capacitance			200			200	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz	
18		C_{rss} Common-Source Reverse Transfer Capacitance			25			25			
19		C_{OSS} Common-Source Output Capacitance			100			100			
20		$t_{d(on)}$ Turn-ON Delay Time			15			15	nsec	V_{DD} = 34V, R_L = 15 ohms, R_G = 25 ohms, $V_{G(on)}$ = 10V	
21		t_r Rise Time			25			25			
22		$t_{d(off)}$ Turn-OFF Delay Time			25			25			
23		t_f Fall Time			20			20			
24	DIODE	I_S Continuous Source Current(1)	3.0			3.5			A		
25		I_{SM} Peak Source Current(1)	8.0			8.0					
26		V_{SD} Source-Drain(1) Forward Voltage			2.0				V	V_{GS} = 0	I_S = 3.0A
27								2.0			I_S = 3.5A

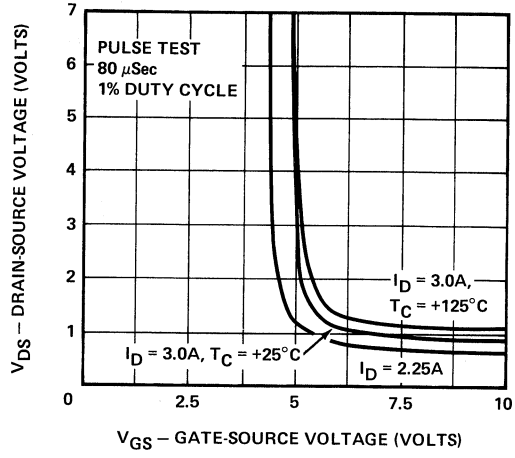
Note 1: Pulse Test 80μSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

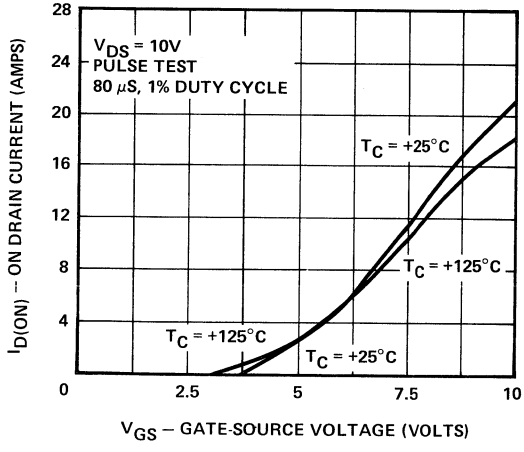
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



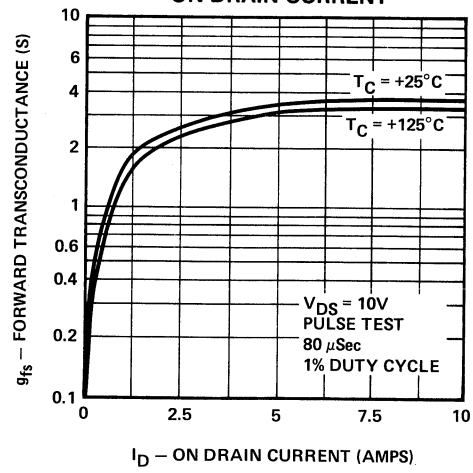
ON VOLTAGE CHARACTERISTICS



ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD5000, SD5001, SD5002

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET ANALOG SWITCH ARRAYS

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD5000	SD5001	SD5002	UNITS
V_{DS}	+20	+10	+15	Vdc
V_{SD}	+20	+10	+15	Vdc
V_{DB}	+25	+15	+22.5	Vdc
V_{SB}	+25	+15	+22.5	Vdc
V_{GS}	−25	−15	−22.5	Vdc
	+30	+25	+30	Vdc
V_{GB}	−0.3	−0.3	−0.3	Vdc
	+30	+25	+30	Vdc
V_{GD}	−25	−15	−22.5	Vdc
	+30	+25	+30	Vdc

I_D Continuous Drain Current 50mA

P_D Total Package Power Dissipation (at or below T_A = +25°C) 640mW

Linear Derating Factor ..... 10.67mW/°C

P_D Single Device Power Dissipation (at or below T_A = +25°C) 300mW

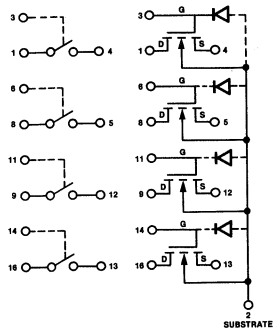
T_j Operating Junction Temperature Range ..... −55 to +85°C

T_S Storage Temperature Range .. −55 to +150°C

ORDERING INFORMATION

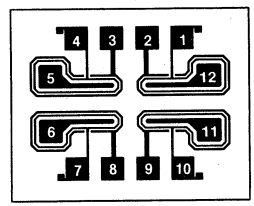
Sorted Chips in Carriers	SD5000CHP	SD5001CHP	SD5002CHP
Ceramic Dual In-Line Package	SD5000J	SD5001J	SD5002J
Plastic Dual In-Line Package	SD5000N	SD5001N	SD5002N

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

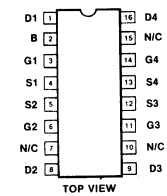
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

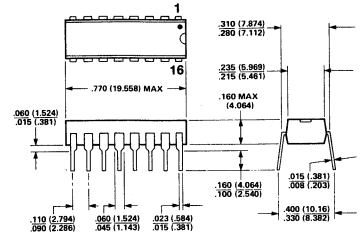
Dimensions: .040 x .032 x .013 inches

PIN CONFIGURATION



PACKAGE DIMENSIONS

Plastic "N" Package



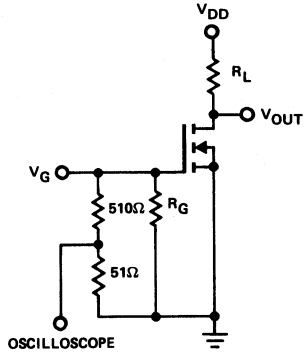
All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER		SD5000			SD5001			SD5002			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20	25		10	25		15	25		V	I_D = 10nA $V_{GS} = V_{BS}$ = −5V	
2		BV_{SD}	Source-Drain Breakdown Voltage	20			10			15			V	I_S = 10nA $V_{GD} = V_{BD}$ = −5V	
3		BV_{DB}	Drain-Substrate Breakdown Voltage	25			15			22.5			V	I_D = 10nA, V_{GB} = 0 Source Open	
4		BV_{SB}	Source-Substrate Breakdown Voltage	25			15			22.5			V	I_S = 10μA, V_{GB} = 0 Drain Open	
5		$I_{D(off)}$	Drain-Source Off Current						10				nA	V_{DS} = 10V	$V_{GS} = V_{BS}$ = −5V
6												10	nA	V_{DS} = 15V	
7						10							nA	V_{DS} = 20V	
8		$I_{S(off)}$	Source-Drain OFF Current						10				nA	V_{SD} = 10V	$V_{GD} = V_{BD}$ = −5V
9												10	nA	V_{SD} = 15V	
10						10							nA	V_{SD} = 20V	
11		I_{GBS}	Gate-Body Leakage Current						1.0				μA	V_{GB} = 25V	$V_{DB} = V_{SB}$ = 0
12						1.0						1.0		V_{GB} = 30V	
13		$V_{GS(th)}$	Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	$V_{DS} = V_{GS}$, I_D = 1μA V_{SB} = 0	
14		$r_{DS(on)}$	Drain-Source ON Resistance		50	70		50	70		50	70	ohms	V_{GS} = 5V	I_D = 1mA V_{SB} = 0
15					30			30			30			V_{GS} = 10V	
16					23			23			23			V_{GS} = 15V	
17					19			19			19			V_{GS} = 20V	
18		r_{DSM}	ON Resistance Match		1.0	5.0		1.0	5.0		1.0	5.0		V_{GS} = 5V	
19	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, VSB = 0	
20		$c_{(gs + gd + gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V $V_{GS} = V_{BS}$ = −15V f = 1MHz	
21		$c_{(gs + db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5			
22		$c_{(gs + sb)}$	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0			
23		$c_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5			
24		C_T	Cross Talk		−107			−107			−107		dB	f = 3KHz, R_G = 600Ω	
25		$t_{d(on)}$	Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	V_{DD} = 5V, $V_{G(on)}$ = 10V R_L = 680Ω, R_G = 51Ω	
26		t_r	Rise Time		0.8	1.0		0.8	1.0		0.8	1.0			
27		t_{off}	Turn OFF Time		10			10			10				

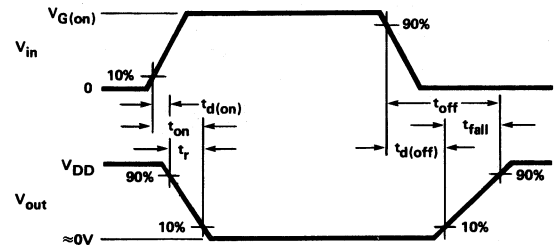
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

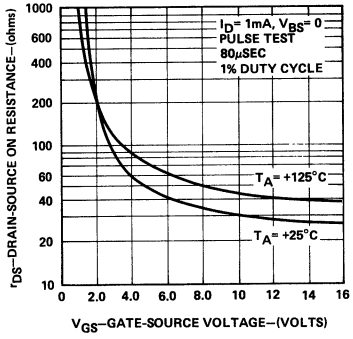
SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS

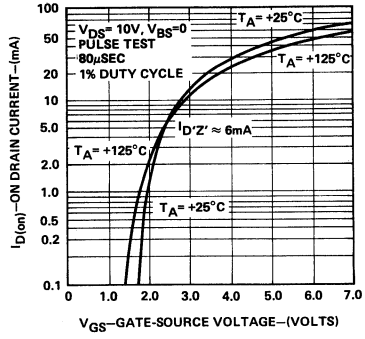


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

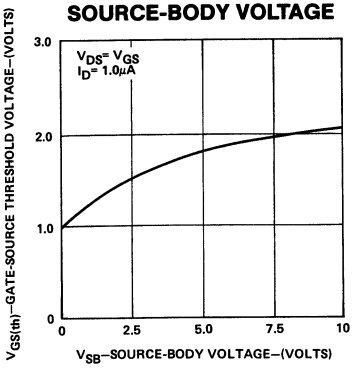
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



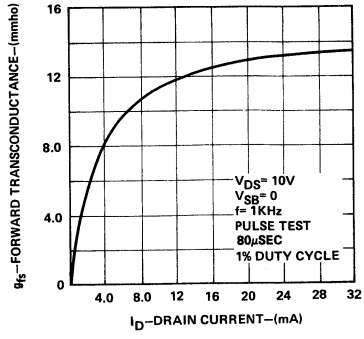
ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE —vs— SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD5100, SD5101

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET ANALOG SWITCH ARRAYS

Common-Source Connected Versions of SD5000

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD5100	SD5101	UNITS
V_{DS}	+30	+15	Vdc
V_{SD}	+0.5	+0.5	Vdc
V_{DB}	+30	+15	Vdc
V_{SB}	+0.5	+0.5	Vdc
V_{GS}	+20	+20	Vdc
V_{GB}	+20	+20	Vdc
	−0.3	−0.3	Vdc
V_{GD}	+20	+20	Vdc
	−30	−15	Vdc

I_D Continuous Drain Current 50mA

P_D Total Package Power Dissipation (at or below T_A = +25°C) 640mW

Linear Derating Factor ..... 10.67mW/°C

P_D Single Device Power Dissipation (at or below T_A = +25°C) 300mW

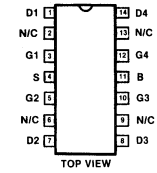
T_j Operating Junction Temperature Range ..... −55 to +85°C

T_S Storage Temperature Range .. −55 to +150°C

ORDERING INFORMATION

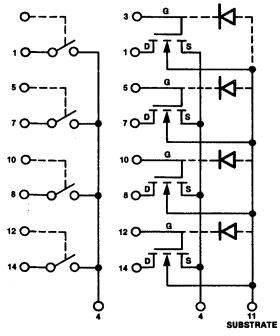
Sorted Chips in Carriers	SD5100CHP	SD5101CHP
Plastic Dual In-Line Package	SD5100N	SD5101N

PIN CONFIGURATION



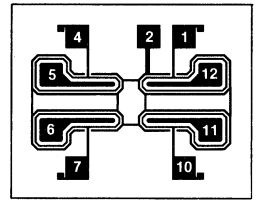
TOP VIEW

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

CHIP CONFIGURATION

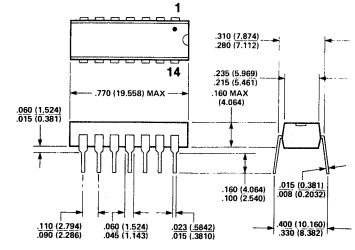


PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source	10	Gate No. 4
4	Gate No. 2	11	Drain No. 4
5	Drain No. 2	12	Drain No. 1
6	Drain No. 3		

Dimensions: .040 x .032 x .013 inches

PACKAGE DIMENSIONS

Plastic "N" Package



All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD5100			SD5101			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	30	35		15	30		V	I_D = 1.0μA, V_{GS} = V_{BS} = 0
2		BV_{SD}	Source-Drain Breakdown Voltage	0.5			0.5			V	I_S = 10nA, V_{GD} = V_{BD} = 0
3		BV_{DB}	Drain-Substrate Breakdown Voltage	30			15			V	I_D = 1.0μA, V_{GB} = 0 Source Open
4		BV_{SB}	Source-Substrate Breakdown Voltage	0.5			0.5			V	I_S = 100nA, V_{GB} = 0 Drain Open
5		$I_{D(off)}$	Drain-Source OFF Current		1.0	10		1.0	10	nA	V_{DS} = 10V, V_{GS} = V_{BS} = 0
6		I_{GBS}	Gate-Substrate Leakage Current			10			10	μA	V_{GS} = 20V, V_{DB} = V_{SB} = 0
7		$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	0.5	1.0	2.0	V	I_D = 1.0μA, V_{DS} = V_{GS} V_{SB} = 0
8		$r_{DS(on)}$	Drain-Source ON Resistance		50	70		50	70	ohms	V_{GS} = 5V; I_D = 1mA, V_{SB} = 0
9					30	45		30	45	ohms	V_{GS} = 10V
10					23			23		ohms	V_{GS} = 15V
11					19			19		ohms	V_{GS} = 20V
12		r_{DSM}	ON Resistance Match		1.0	5.0		1.0	5.0	ohms	V_{GS} = 5V
13	DYNAMIC	g_{fs}	Common-Source Forward Transcond	10	15		10	15		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, V_{SB} = 0
14		$C_{(gs+gd+gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V V_{GS} = V_{BS} = −5V f = 1MHZ
15		$C_{(gd+db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		
16		C_{dg}	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		
17		C_T	Cross Talk		−107			−107		dB	f = 3KHz, R_G = 600Ω

TOPAZ SEMICONDUCTOR

SD5200

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET DRIVER ARRAY

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

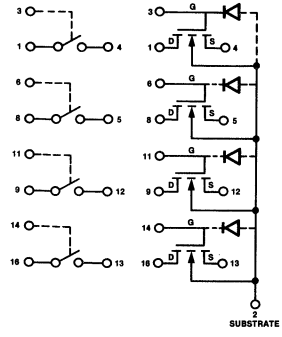
V_{DS} Drain-Source Voltage ..... +30Vdc
V_{SD} Source-Drain Voltage ..... +0.5Vdc
V_{DB} Drain-Body Voltage ..... +30Vdc
V_{SB} Source-Body Voltage ..... +15Vdc
V_{GS} Gate-Source Voltage ..... +25Vdc
V_{GB} Gate-Body Voltage ..... +25Vdc
Gate-Body Voltage ..... −0.3Vdc
V_{GD} Gate-Drain Voltage ..... +25Vdc
I_D Continuous Drain Current 50mA

P_D Total Package Power Dissipation (at or below T_A = +25°C) 640mW
Linear Derating Factor ..... 10.7mW/°C
P_D Single Device Power Dissipation (at or below T_A = +25°C) 300mW
Linear Derating Factor ..... 5.0mW/°C
T_j Operating Junction Temperature Range ..... −55 to +85°C
T_S Storage Temperature Range .. −55 to +150°C

ORDERING INFORMATION

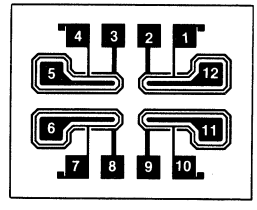
Sorted Chips in Carriers	SD5200CHP
Plastic Dual In-Line Package	SD5200N

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

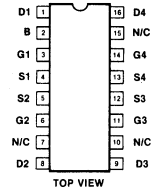
CHIP CONFIGURATION



PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

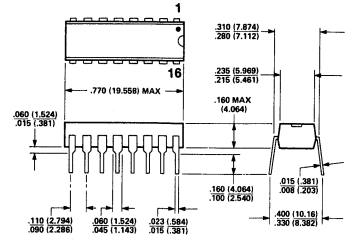
Dimensions: .040 x .032 x .013 inches

PIN CONFIGURATION



PACKAGE DIMENSIONS

Plastic "N" Package



All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SD5200 MIN	SD5200 TYP	SD5200 MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	30	35		V	$I_D = 10\mu A, V_{GS} = V_{BS} = 0$
2	STATIC	BV_{SB}	Source-Substrate Breakdown Voltage	15			V	$I_S = 10\mu A$, $V_{GB} = 0$ Drain Open
3	STATIC	I_{GBS}	Gate-Body Leakage Current			1.0	μA	$V_{GB} = 25V, V_{DB} = V_{SB} = 0$
4	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	V	$V_{DS} = V_{GS}, I_D = 1.0\mu A$ $V_{SB} = 0$
5	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		50	80	ohms	$V_{GS} = 5V$
6	STATIC				30		ohms	$V_{GS} = 10V$
7	STATIC				23		ohms	$V_{GS} = 15V$
8	STATIC				19		ohms	$V_{GS} = 20V$
								$I_D = 1mA$ $V_{SB} = 0$
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10	12		mmhos	$V_{DS} = 10V, I_D = 20mA$ $f = 1KHz, V_{SB} = 0$
10	DYNAMIC	$C_{(gs + gd + gb)}$	Gate Node Capacitance		2.4	3.5	pF	$f = 1MHz$ $V_{DS} = 10V$ $V_{GS} = V_{BS} = -15V$
11	DYNAMIC	$C_{(gd + db)}$	Drain Node Capacitance		1.3	1.5	pF	
12	DYNAMIC	$C_{(gs + sb)}$	Source Node Capacitance		3.5	4.0	pF	
13	DYNAMIC	$C_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5	pF	
14	DYNAMIC	C_T	Cross Talk		−107		dB	

TOPAZ SEMICONDUCTOR

SD5400, SD5401, SD5402

QUAD D-MOS FET ANALOG SWITCH ARRAYS

ORDERING INFORMATION

14 Pin Plastic, Small-Outline Package	SD5400CY	SD5401CY	SD5402CY
Description	20V, 30Ω	10V, 30Ω	15V, 30Ω
Temperature Range	Commercial	Commercial	Commercial

FEATURES

- Low Interelectrode Capacitances
  - Analog Input—3.5pF typ.
  - Input (Gate) —2.4pF typ.
  - Output —1.3pF typ.
  - Feedback —0.3pF typ.
- Low Insertion Loss, r_{DS} <30 ohms
- Low Crosstalk—-107dB @ 3KHz
- Bidirectional Switches
- Small-Outline Surface Mount Package

APPLICATIONS

- High Speed Analog Switches
  - Analog Range ± 10V—SD5400
  - Analog Range ±7.5V—SD5402
  - Analog Range ±5.0V—SD5401
- High-Speed Switch Drivers
  - 20V—SD5400
  - 15V—SD5402
  - 10V—SD5401
- Sample & Hold

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

PARAMETER	SD5400	SD5401	SD5402	UNITS
V_{DS}	+20	+10	+15	V
V_{SD}	+20	+10	+15	V
V_{DB}	+25	+15	+22.5	V
V_{SB}	+25	+15	+22.5	V
V_{GS}	-25	-15	-22.5	V
	+30	+25	+30	V
V_{GB}	-0.3	-0.3	-0.3	V
	+30	+25	+30	V
V_{GD}	-25	-15	-22.5	V
	+30	+25	+30	V

I_D Continuous Drain Current 50mA

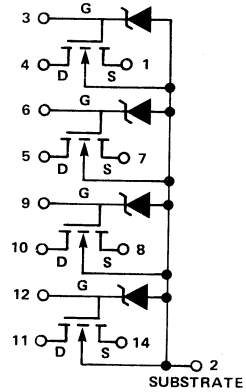
P_D Total Package Power Dissipation
(at or below T_A = +25°C) 640mW
Linear Derating Factor ..... 5.33mW/°C

P_D Single Device Power Dissipation
(at or below T_A = +25°C) 300mW

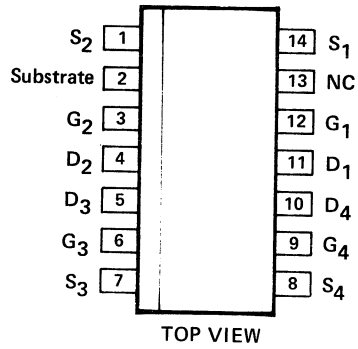
T_J Operating Junction
Temperature Range ..... 0 to +70°C

T_S Storage Temperature Range ..... -55 to +125°C

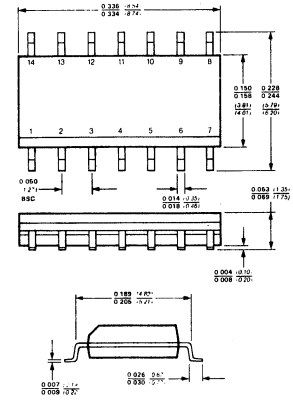
SCHEMATIC DIAGRAM



PIN CONFIGURATION



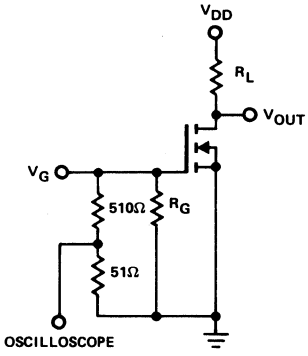
PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise noted)

#		PARAMETER		SD5400			SD5401			SD5402			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20	25		10	25		15	25		V	I_D = 10nA $V_{GS} = V_{BS} = -5V$	
2		BV_{SD}	Source-Drain Breakdown Voltage	20			10			15			V	I_S = 10nA $V_{GD} = V_{BD} = -5V$	
3		BV_{DB}	Drain-Substrate Breakdown Voltage	25			15			22.5			V	I_D = 10nA, V_{GB} = 0 Source Open	
4		BV_{SB}	Source-Substrate Breakdown Voltage	25			15			22.5			V	$I_S = 10\mu A, V_{GB} = 0$ Drain Open	
5		$I_{D(off)}$	Drain-Source Off Current						10				nA	V_{DS} = 10V	$V_{GS} = V_{BS} = -5V$
6												10	nA	V_{DS} = 15V	
7						10							nA	V_{DS} = 20V	
8		$I_{S(off)}$	Source-Drain OFF Current						10				nA	V_{SD} = 10V	$V_{GD} = V_{BD} = -5V$
9												10	nA	V_{SD} = 15V	
10						10							nA	V_{SD} = 20V	
11		I_{GBS}	Gate-Body Leakage Current						1.0				μ A	V_{GB} = 25V	$V_{DB} = V_{SB} = 0$
12						1.0						1.0		V_{GB} = 30V	
13		$V_{GS(th)}$	Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	$V_{DS} = V_{GS}, I_D = 1\mu A$ V_{SB} = 0	
14		$r_{DS(on)}$	Drain-Source ON Resistance		50	70		50	70		50	70	ohms	V_{GS} = 5V	I_D = 1mA V_{SB} = 0
15					30			30			30			V_{GS} = 10V	
16					23			23			23			V_{GS} = 15V	
17					19			19			19			V_{GS} = 20V	
18		r_{DSM}	ON Resistance Match		1.0	5.0		1.0	5.0		1.0	5.0		V_{GS} = 5V	
19	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, VSB = 0	
20		$c_{(gs + gd + gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V $V_{GS} = V_{BS} = -15V$ f = 1MHz	
21		$c_{(gs + db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5			
22		$c_{(gs + sb)}$	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0			
23		$c_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5			
24		C_T	Cross Talk		−107			−107			−107		dB	f = 3KHz, R_G = 600Ω	
25		$t_{d(on)}$	Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	V_{DD} = 5V, $V_{G(on)}$ = 10V R_L = 680Ω, R_G = 51Ω	
26		t_r	Rise Time		0.8	1.0		0.8	1.0		0.8	1.0			
27		t_{off}	Turn OFF Time		10			10			10				

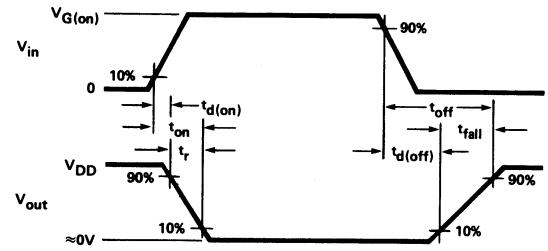
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
t_r < 0.5 nSEC
PULSE WIDTH – 100 nSEC

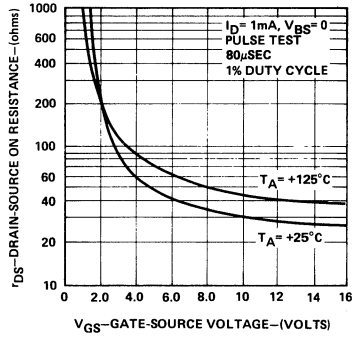
SAMPLING OSCILLOSCOPE
t_r < 0.36 nSEC
R_{in} > 1MΩ
C_{in} < 2.0 pF

TEST WAVEFORMS

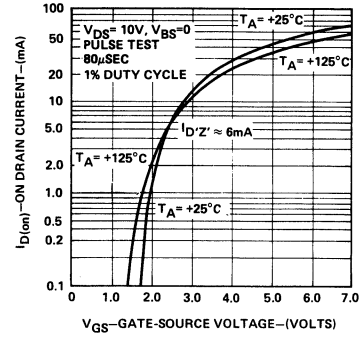


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

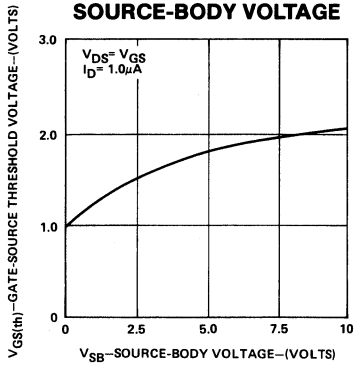
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



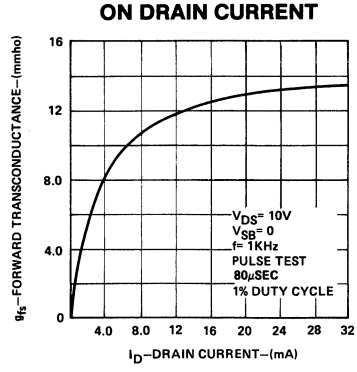
ON DRAIN CURRENT —vs— GATE-SOURCE VOLTAGE



GATE-SOURCE THRESHOLD VOLTAGE —vs— SOURCE-BODY VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

SD5501

N-CHANNEL DEPLETION-MODE 4-CHANNEL D-MOS FET ARRAY

FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Wide Dynamic Range

APPLICATIONS

- High-Speed Analog Switches
- Wide-Band Dual Differential Amplifiers
- Dual Cascode Amplifiers
- High Intercept Point Double Balanced Mixers

ABSOLUTE MAXIMUM RATINGS (per channel,

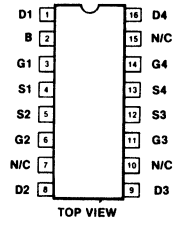
T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage	+20V
V_{SD} Source-Drain Voltage	+10V
V_{DB} Drain-Body Voltage	+25V
V_{SB} Source-Body Voltage	+15V
V_{GD} Gate-Drain Voltage	+25V
V_{GS} Gate-Source Voltage	+25V
V_{GB} Gate-Body Voltage	+25V
V_{G-G} Gate-to-Gate Voltage	+25V
V_{D-D} Drain-to-Drain Voltage	+25V
V_{S-S} Source-to-Source Voltage	+15V
I_D Continuous Drain Current	+50 mA
P_D Device Dissipation (per channel)	300 mW
Derating Factor	2.4 mW/°C
P_D Total Device Dissipation	640 mW
Derating Factor	5.12 mW/°C
T_j Operating Junction Temperature Range	-55 to +150°C
T_S Storage Temperature Range	-55 to +150°C
T_L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260°C

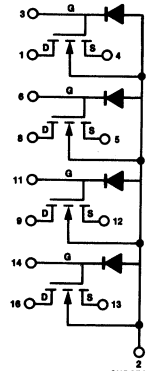
ORDERING INFORMATION

Description	Sorted Chips in Carriers	Ceramic Dual In-Line Package	Plastic Dual In-Line Package
20V, 150Ω	SD5501CHP	SD5501J	SD5501N

PIN CONFIGURATION

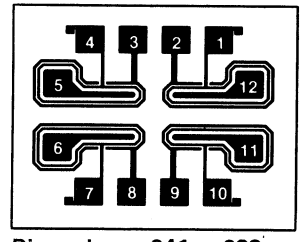


SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

CHIP CONFIGURATION

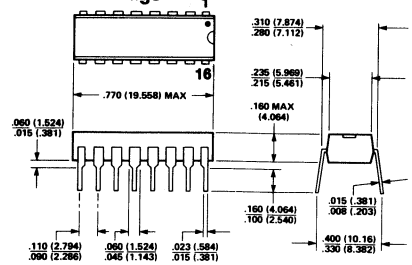


Dimensions: .041 x .033 x .013 inches

PAD NO.	PAD FUNCTION
1	Gate No. 1
2	Source No. 1
3	Source No. 2
4	Gate No. 2
5	Drain No. 2
6	Drain No. 3
7	Gate No. 3
8	Source No. 3
9	Source No. 4
10	Gate No. 4
11	Drain No. 4
12	Drain No. 1

PACKAGE DIMENSIONS

Plastic "N" Package



All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (per channel, T_A = +25°C, unless otherwise noted)

#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20			V	I_D = 10nA, V_{GS} = V_{BS} = -5V	
2		BV_{SD}	Source-Drain Breakdown Voltage	10				I_S = 10nA, V_{GD} = V_{BD} = -5V	
3		BV_{DB}	Drain-Body Breakdown Voltage	25				I_D = 10nA, V_{GB} = 0 Source Open	
4		BV_{SB}	Source-Body Breakdown Voltage	15				I_S = 10μA, V_{GB} = 0 Drain open	
5		$I_{GSS(fwd)}$	Forward Gate Leakage Current			1.0	nA	V_{GS} = 25V, V_{DS} = V_{BS} = 0	
6		I_G	Gate Operating Current		-3.0	-100	pA	V_{DG} = 20V, I_D = 5.0 mA, V_{BS} = -5.6V	
7					-0.7	-10	nA		T_A = +125°C
8		$V_{GS\ (off)}$	Gate-Source Cutoff Voltage	-1.0		-5.0	V	V_{DS} = 10V, I_D = 1.0μA, V_{BS} = -5.6V	
9		$V_{GS(on)}$	Gate-Source ON Voltage	-0.3		-3.0		V_{DG} = 10V, I_D = 5mA, V_{SB} = -5.6V	
10		I_{DSX}	Zero Gate Voltage[1] Drain Current	7.0		40	mA	V_{DS} = 10V, V_{GS} = 0, V_{BS} = -5.6V	
11				5.0					T_A = +125°C
12		$r_{DS(ON)}$	Drain-Source ON Resistance		100	150	ohms	I_D = 1.0mA, V_{GS} = 0, V_{BS} = -5.6V	
13	DYNAMIC	g_{fs}	Common-Source[1] Forward Transconductance	5.0	7.5	10	mmhos	V_{DG} = 10V, I_D = 5.0 mA, V_{BS} = -5.6V	f = 1 KHz
14		g_{os}	Common-Source Output Conductance		200	300	μmhos		
15		C_{iss}	Common-Source Input Capacitance		3.5		pF		f = 1 MHz
16		C_{oss}	Common-Source Output Capacitance		1.2				
17		C_{rss}	Common-Source Reverse Transfer Capacitance		0.3				
18		$C_{(gs\ +\ sb)}$	Source Node Capacitance		4.5				
19	MATCHING	V_{GSM}	Gate Source[2] Voltage Match		50		mV		
20		$r_{DS(on)}$	Drain-Source[1], [2] ON Resistance Match	0.90	0.98	1.0		I_D = 1.0 mA, V_{GS} = 0, V_{BS} = 5.6V	
21		I_{DSXM}	Zero Gate Voltage[1], [2] Drain Current Match	0.90		1.0		V_{DG} = 10V, I_D = 5.0 mA, V_{BS} = -5.6V	
22		g_{fsm}	Transconductance Match[1], [2]	0.90		1.0			f = 1 KHz

Note 1: Pulse Test, 80μsec, 1% Duty Cycle
Note 2: Match of 4 channels

TYPICAL PERFORMANCE CHARACTERISTICS: SEE TZ5911

TOPAZ SEMICONDUCTOR

TZ402

N-CHANNEL ENHANCEMENT-MODE D-MOS FET ULTRA HIGH-SPEED LOW-COST SWITCH

FEATURES

- Reliable, low cost, plastic package
- High Speed Switching, tr < 1nSec
- Low Capacitance, c_{rss} 0.3 pF typ
- CMOS and TTL Compatible Input

APPLICATIONS

- Switch Drivers
- Video Switches
- Sample and Hold and Track and Hold
- VHF/UHF Amplifiers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Drain-Source Voltage ..... +15V
Gate-Source Voltage ..... -0.3V
+20V
Gate-Drain Voltage ..... -0.3V
+20V
Source-Drain Voltage ..... -0.3V

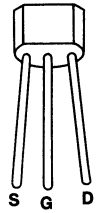
Continuous Drain Current 50mA
Power Dissipation (at or below T_A = +25°C) 300mW
Linear Derating Factor ..... 3.0mW/°C
Operating Storage and
Junction Temperature Range -40°C to +

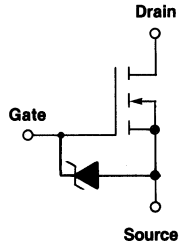
ORDERING INFORMATION

TO-92 Plastic Package	TZ402BD
Description	15V, 80 ohm

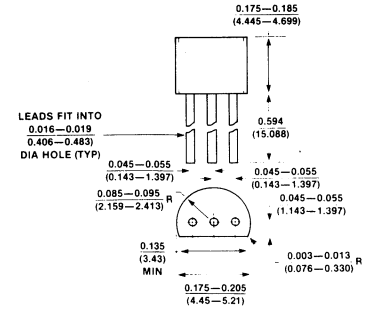
PIN CONFIGURATION/SCHEMATIC DIAGRAM

TO-92





PACKAGE DIMENSIONS TO-92



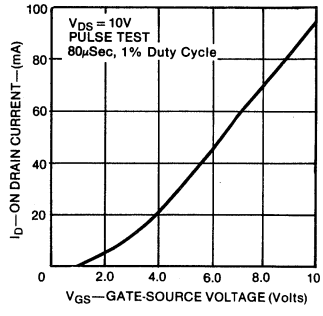
All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

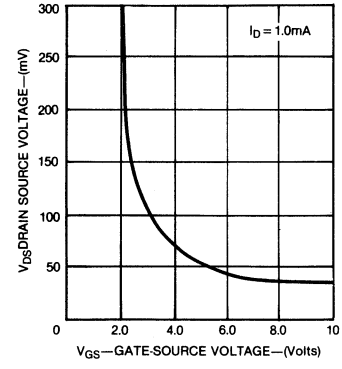
	CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION
STATIC	BV_{DS}	Drain-Source Breakdown Voltage	15	25		V	I_D = 1.0μA, V_{GS} = 0
	$I_{D(off)}$	Drain-Source OFF Leakage Current			1.0	μA	V_{DS} = 15V, V_{GS} = 0
	I_{GSS}	Gate-Source Leakage Current			1.0	μA	V_{GS} = 20V, V_{DS} = 0
	$I_{D(on)}$	Drain-Source ON Current	50	100		mA	V_{DS} = 10V, V_{GS} = 10V Pulse Test
	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.7		1.5	V	I_D = 1.0μA, V_{DS} = V_{GS}
	$V_{DS(on)}$	Drain-Source ON Voltage		150	250	mV	I_D = 1mA, V_{GS} = 2.4V
	$r_{DS(on)}$	Drain-Source ON Resistance		150	250	ohms	
	$V_{DS(on)}$	Drain-Source ON Voltage		60	80	mV	I_D = 1mA, V_{GS} = 4.5V
	$r_{DS(on)}$	Drain-Source ON Resistance		60	80	ohms	
	g_{fs}	Common-Source Forward Transcond.	8.0	12		mmhos	I_D = 20mA V_{DS} = 10V f = 1KHz Pulse Test
DYNAMIC	c_{iss}	Common-Source Input Capacitance		4.0	5.0		V_{DS} = 10V, V_{GS} = 0 f = 1MHz
	c_{oss}	Common-Source Output Capacitance		1.8	2.5	pf	
	c_{rss}	Common-Source Reverse Transfer Capacitance		0.3	0.5		
	$t_{d(on)}$	Turn ON Delay Time		0.7	1.0		V_{DD} = 10V, R_L = 680Ω
	t_r	Rise Time		0.8	1.0	nS	$V_{G(on)}$ = 10V, R_G = 51Ω
	$t_{(off)}$	Turn OFF Time		12			C_L = 1.5pF

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise noted)

ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



DRAIN-SOURCE ON VOLTAGE —VS— GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

TZ403

N-CHANNEL ENHANCEMENT-MODE D-MOS FET ULTRA HIGH-SPEED LOW-COST SWITCH

ORDERING INFORMATION

TO-92 Plastic Package	TZ403BD
Description	15V, 60 ohm

FEATURES

- Reliable, Low Cost, Plastic Package
- High Speed Switching, tr < 1nSec
- Low Capacitance, c_{rss} 0.4pF typ
- CMOS and TTL Compatible Input

APPLICATIONS

- Switch Drivers
- Video Switches
- Sample Hold and Track and Hold
- VHF/UHF Amplifiers

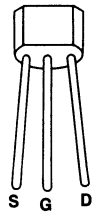
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

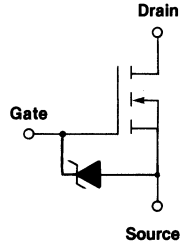
Drain-Source Voltage ..... +15V
Gate-Source Voltage ..... -0.3V
+20V
Gate-Drain Voltage ..... -0.3V
+20V
Source-Drain Voltage ..... -0.3V

Continuous Drain Current 50mA
Power Dissipation (at or below T_A = +25°C) 300mW
Linear Derating Factor ..... 3.0mW/°C
Operating Storage and
Junction Temperature Range -40°C to +125°C

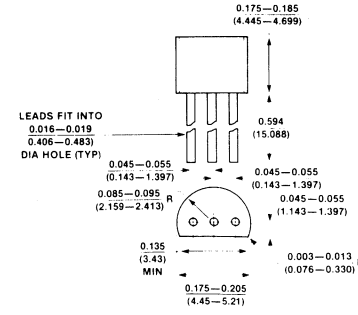
PIN CONFIGURATION/SCHEMATIC DIAGRAM

TO-92





PACKAGE DIMENSIONS TO-92

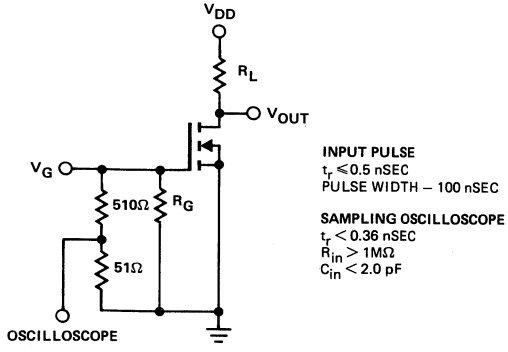


All dimensions in inches and (millimeters)

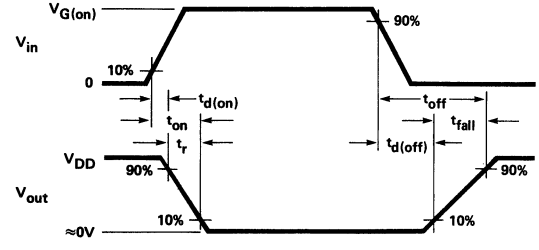
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

	CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION
STATIC	BV_{DS}	Drain-Source Breakdown Voltage	15	25		V	I_D = 1.0μA, V_{GS} = 0
	$I_{D(off)}$	Drain-Source OFF Leakage Current			1.0	μA	V_{DS} = 15V, V_{GS} = 0
	I_{GSS}	Gate-Source Leakage Current			1.0	μA	V_{GS} = 20V, V_{DS} = 0
	$I_{D(on)}$	Drain-Source ON Current	80	120		mA	V_{DS} = 10V, V_{GS} = 10V Pulse Test
	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.7		1.5	V	I_D = 1.0μA, V_{DS} = V_{GS}
	$V_{DS(on)}$	Drain-Source ON Voltage		140	175	mV	I_D = 1mA, V_{GS} = 2.4V
	$r_{DS(on)}$	Drain-Source ON Resistance		140	175	ohms	
	$V_{DS(on)}$	Drain-Source ON Voltage		40	60	mV	I_D = 1mA, V_{GS} = 4.5V
	$r_{DS(on)}$	Drain-Source ON Resistance		40	60	ohms	
DYNAMIC	g_{fs}	Common-Source Forward Transcond.	15	19		mmhos	I_D = 20mA V_{DS} = 10V f = 1KHz Pulse Test
	c_{iss}	Common-Source Input Capacitance		4.5	6.0	pf	V_{DS} = 10V, V_{GS} = 0 f = 1MHz
	c_{oss}	Common-Source Output Capacitance		2.0	3.0		
	c_{rss}	Common-Source Reverse Transfer Capacitance		0.4	0.6		
	$t_{d(on)}$	Turn ON Delay Time		0.8	1.2	nS	V_{DD} = 10V, R_L = 680Ω $V_{G(on)}$ = 10V, R_G = 51Ω C_L = 1.5pF
	t_r	Rise Time		0.9	1.2		
	$t_{(off)}$	Turn OFF Time		14			

SWITCHING TIMES TEST CIRCUIT

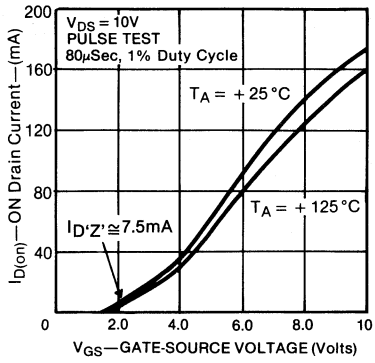


TEST WAVEFORMS

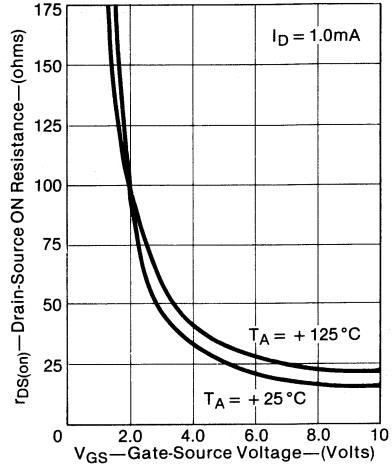


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

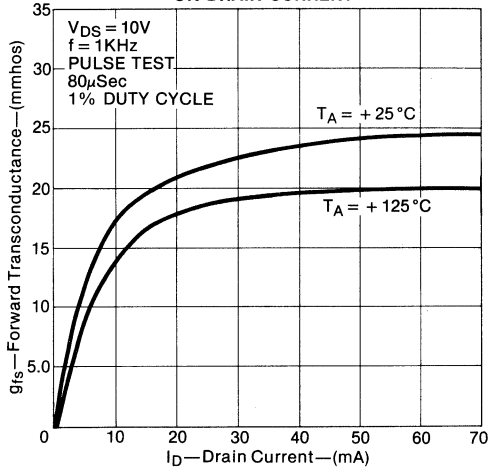
ON DRAIN CURRENT
—VS—
GATE SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

TZ404

N-CHANNEL ENHANCEMENT-MODE D-MOS FET ULTRA HIGH-SPEED LOW-COST SWITCH

ORDERING INFORMATION

TO-92 Plastic Package	TZ404BD
Description	20V, 20 ohm

FEATURES

- Reliable, Low Cost, Plastic Package
- High Speed Switching, tr < 2nSec
- Low Capacitance, c_{rss} 1.2 pF typ
- CMOS and TTL Compatible Input

APPLICATIONS

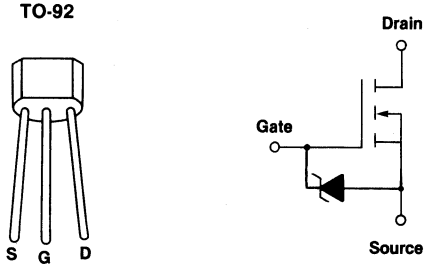
- Switch Drivers
- Video Switches
- Sample Hold and Track and Hold
- VHF/UHF Amplifiers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

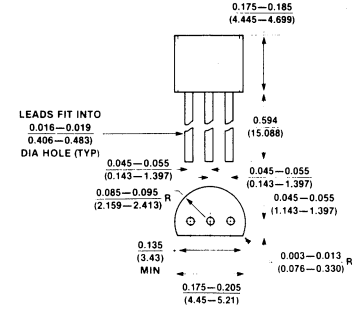
Drain-Source Voltage ..... +20V
Gate-Source Voltage ..... -0.3V
+20V
Gate-Drain Voltage ..... -0.3V
+20V
Source-Drain Voltage ..... -0.3V

Peak Pulsed Drain Current ..... +0.8A
Continuous Drain Current 140mA
Power Dissipation (at or below T_A = +25°C) 300mW
Linear Derating Factor ..... 3.0mW/°C
Operating Storage and
Junction Temperature Range -40°C to +125°C

PIN CONFIGURATION/SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS TO-92



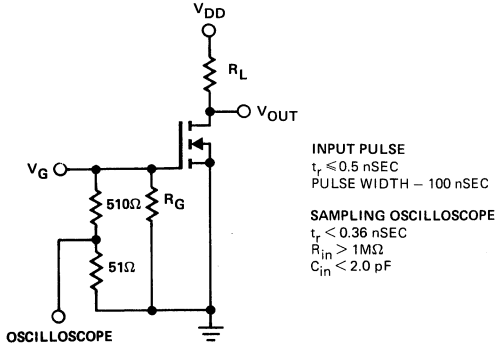
All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

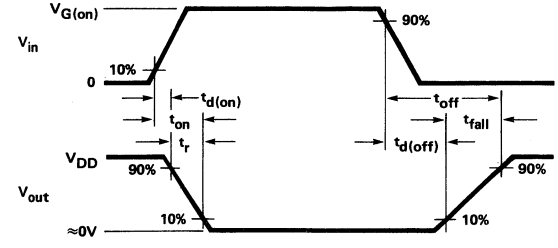
	CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION	
STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20	25		V	I_D = 1.0μA, V_{GS} = 0	
	$I_{D(off)}$	Drain-Source OFF Leakage Current			1.0	μA	V_{DS} = 15V, V_{GS} = 0	
	I_{GSS}	Gate-Source Leakage Current			10	μA	V_{GS} = 20V, V_{DS} = 0	
	$I_{D(on)}$	Drain-Source ON Current	0.8	1.2		A	V_{DS} = 10V, V_{GS} = 10V	(Note 1)
	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.7	1.1	1.5	V	I_D = 1.0μA, V_{DS} = V_{GS}	
	$V_{DS(on)}$	Drain-Source ON Voltage			200	mV	I_D = 10mA	(Note 1)
	$r_{DS(on)}$	Drain-Source ON Resistance			20	ohms	V_{GS} = 2.4V	
	$V_{DS(on)}$	Drain-Source ON Voltage			800	mV	I_D = 100mA	
	$r_{DS(on)}$	Drain-Source ON Resistance			8.0	ohms	V_{GS} = 4.5V	
DYNAMIC	g_{fs}	Common-Source Forward Transcond.	100			mmhos	I_D = 0.3A V_{DS} = 20V f = 1KHz	
	c_{iss}	Common-Source Input Capacitance		12	18	pf	V_{DS} = 20V, V_{GS} = 0 f = 1MHz	
	c_{oss}	Common-Source Output Capacitance		6.0	8.0			
	c_{rss}	Common-Source Reverse Transfer Capacitance		1.2	2.0			
	$t_{d(on)}$	Turn ON Delay Time		1.0	1.5	nS	V_{DD} = 10V, R_L = 390Ω $V_{G(on)}$ = 10V, R_G = 51Ω C_L = 1.5pF	
	t_r	Rise Time		1.0	2.0			
	$t_{(off)}$	Turn OFF Time		10				

Note 1: Pulse Test, 80μSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

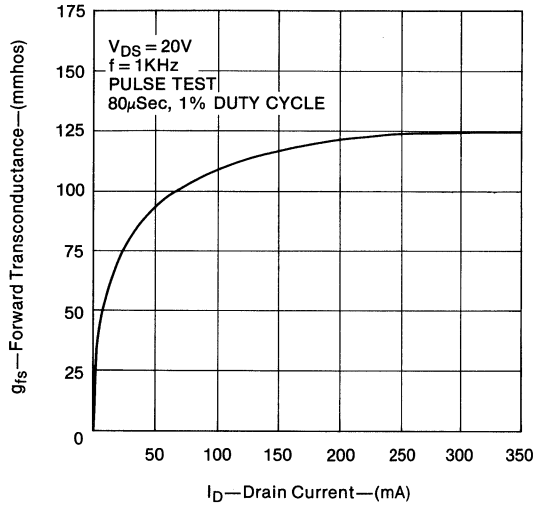


TEST WAVEFORMS

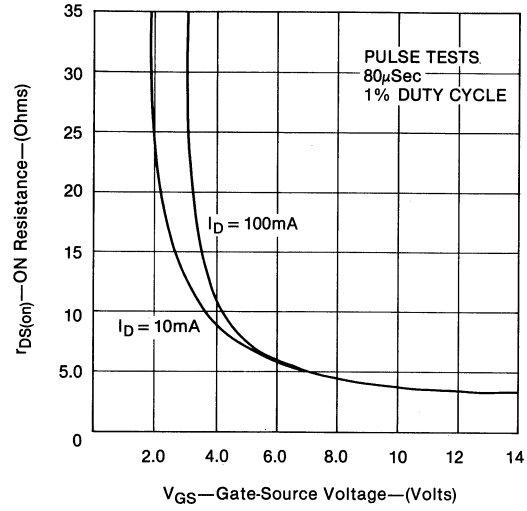


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

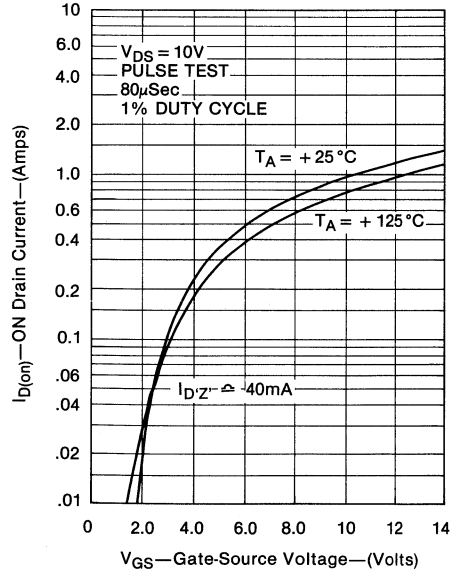
FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

TZ5911

N-CHANNEL DEPLETION-MODE DUAL D-MOS FET

FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Pin and Function Compatible to Industry Standard Dual J-FETs with addition of Substrate Bias Pin

APPLICATIONS

- High-Speed Analog Comparators
- Wide-Band Differential Amplifiers
- Cascode Amplifiers
- High Intercept Point Balanced Mixers

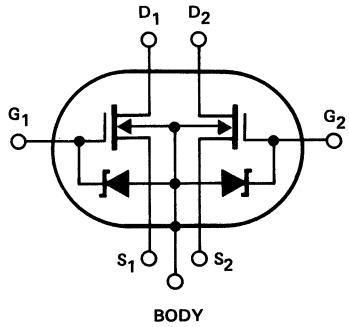
ABSOLUTE MAXIMUM RATINGS (per side, T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage	+20V
V_{SD} Source-Drain Voltage	+10V
V_{DB} Drain-Body Voltage	+25V
V_{SB} Source-Body Voltage	+15V
V_{GD} Gate-Drain Voltage	+25V
V_{GS} Gate-Source Voltage	+25V
V_{GB} Gate-Body Voltage	+25V
V_{G1G2} Gate-to-Gate Voltage	+25V
V_{D1D2} Drain-to-Drain Voltage	+25V
V_{S1S2} Source-to-Source Voltage	+15V
I_D Continuous Drain Current	+50 mA
P_D Device Dissipation (each side)	360 mW
Derating Factor	2.88 mW/°C
P_D Total Device Dissipation	500 mW
Derating Factor	4 mW/°C
T_j Operating Junction Temperature Range	-55 to +150°C
T_S Storage Temperature Range	-55 to +150°C
T_L Lead Temperature (1/16" from mounting surface for 10 sec.)	+260°C

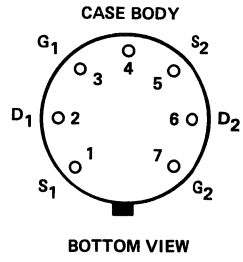
ORDERING INFORMATION

TO-78 Hermetic Package	TZ5911HD

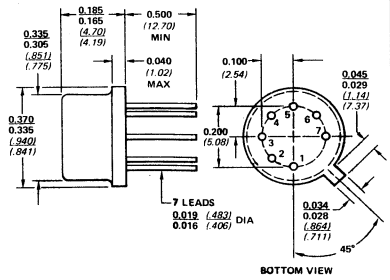
SCHEMATIC DIAGRAM



PIN CONFIGURATION



PACKAGE DIMENSIONS TO-78



All dimensions in inches and (millimeters)

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

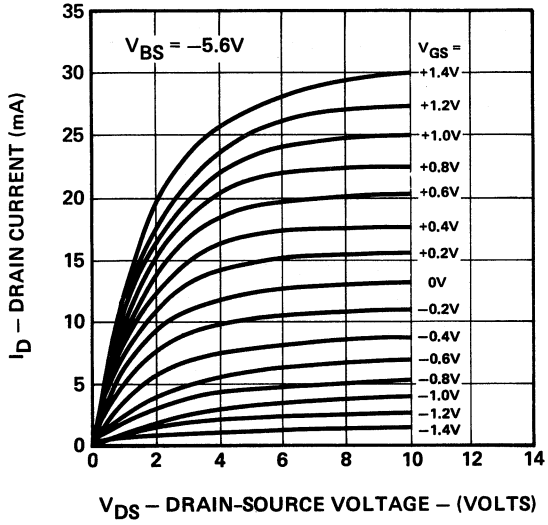
ELECTRICAL CHARACTERISTICS (T_A = +25°C, per side, unless otherwise noted)

#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20			V	I_D = 10nA, V_{GS} = V_{BS} = -5V	
2		BV_{SD}	Source-Drain Breakdown Voltage	10				I_S = 10nA, V_{GD} = V_{BD} = -5V	
3		BV_{DB}	Drain-Body Breakdown Voltage	25				I_D = 10nA, V_{GB} = 0 Source Open	
4		BV_{SB}	Source-Body Breakdown Voltage	15				I_S = 10μA, V_{GB} = 0 Drain open	
5		$I_{GSS(fwd)}$	Forward Gate Leakage Current			1.0	nA	V_{GS} = 25V, V_{DS} = V_{BS} = 0	
6		I_G	Gate Operating Current		-3.0	-100	pA	V_{DG} = 20V, I_D = 5.0 mA, V_{BS} = -5.6V	
7					-0.7	-10	nA	V_{BS} = -5.6V	T_A = +125°C
8		$V_{GS\ (off)}$	Gate-Source Cutoff Voltage	-1.0		-5.0	V	V_{DS} = 10V, I_D = 1.0nA, V_{BS} = -5.6V	
9		$V_{GS(on)}$	Gate-Source ON Voltage	-0.3		-3.0		V_{DG} = 10V, I_D = 5mA, V_{BS} = -5.6V	
10		I_{DSX}	Zero Gate Voltage[1] Drain Current	7.0		40	mA	V_{DS} = 10V, V_{GS} = 0, V_{BS} = -5.6V	
11				5.0				V_{BS} = -5.6V	T_A = +125°C
12		$r_{DS(ON)}$	Drain-Source ON Resistance		100	150	ohms	I_D = 1.0mA, V_{GS} = 0, V_{BS} = -5.6V	
13	DYNAMIC	g_{fs}	Common-Source[1] Forward Transcond.	5.0	7.5	10	mmhos	V_{DG} = 10V, I_D = 5.0 mA, V_{BS} = -5.6V	f = 1 KHz
14		g_{os}	Common-Source Output Conductance		200		μmhos		
15		C_{iss}	Common-Source Input Capacitance		3.5		pF		f = 1 MHz
16		C_{oss}	Common-Source Output Capacitance		1.2				
17		C_{rss}	Common Source Reverse Transfer Capacitance		0.3				
18		$C_{(gs\ +\ sb)}$	Source Node Capacitance		4.5				
19	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate Source Voltage		20		mV	V_{DG} = 10V, I_D = 5.0 mA, V_{BS} = -5.6V	
20		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Differential Drift		20		μV/°C		T_A = -55°C to +125°C
21		$I_{DSX\ 1/2}$	Zero Gate Voltage[1,2] Drain Current Ratio	0.90		1.0			
22		$g_{fs\ 1/2}$	Transcond. Ratio[1,2]	0.90		1.0			f = 1 KHz

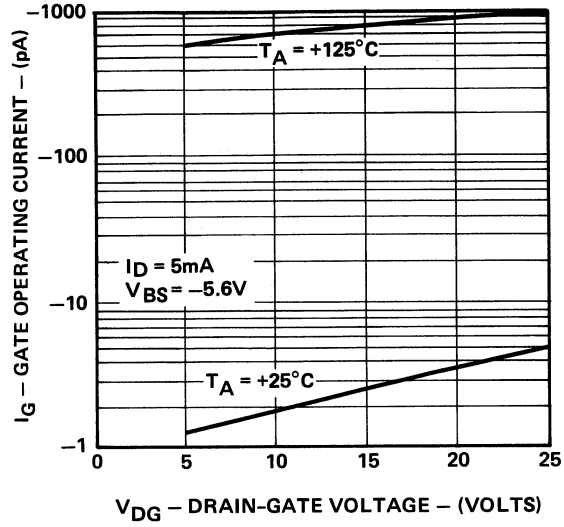
Note 1: Pulse Test, 80μsec, 1% Duty Cycle
Note 2: The lower value is side 1.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per side, unless otherwise specified)

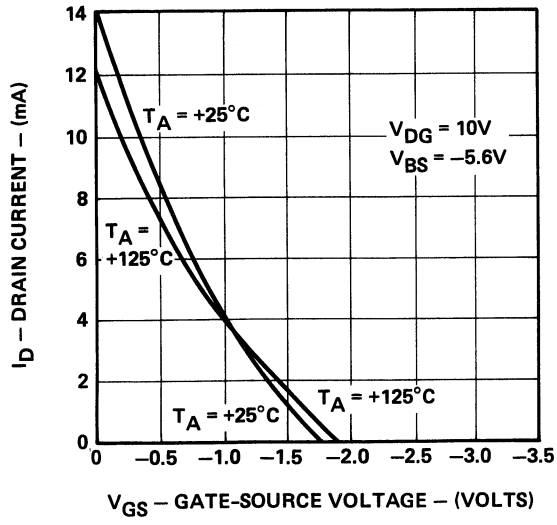
OUTPUT CHARACTERISTIC



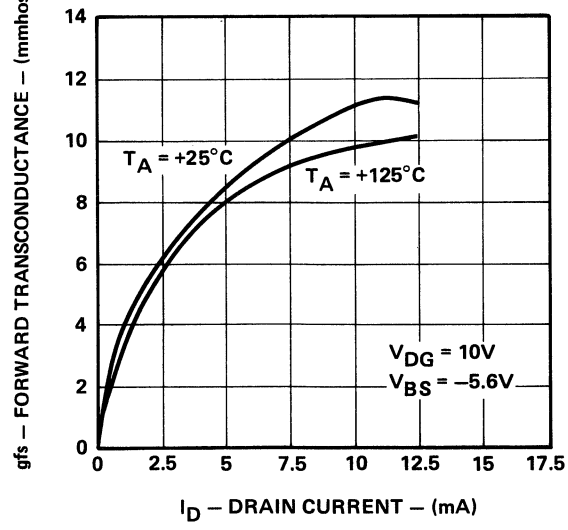
GATE OPERATING CURRENT —VS— DRAIN-GATE VOLTAGE



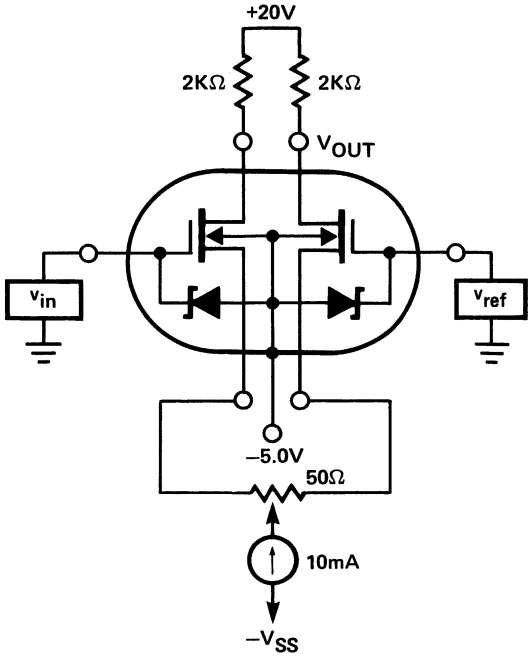
TRANSFER CHARACTERISTIC



FORWARD TRANSCONDUCTANCE —VS— DRAIN CURRENT



DIFFERENTIAL AMPLIFIER/COMPARATOR



PERFORMANCE CHARACTERISTICS (T_A = +25°C)

Low Frequency Differential Voltage Gain—6.2 min., 11.8 typ.

v_{in}, v_{ref} range—-5.0V to +10V

v_{out} max.—+20V

Input Bias Current—100 pA max., 4 pA typ.

Differential Input Bias Current—0.4 pA typ.

Gate Voltages must be positive with respect to Body (Substrate) Voltage at all times.

TOPAZ SEMICONDUCTOR

VN0104, VN0106 VN0109

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-92 Plastic Package	VN0104N3	VN0106N3	VN0109N3
Sorted Chips in Carriers	VN0104ND	VN0106ND	VN0109ND
Description	40V, 3.0 ohm	60V, 3.0 ohm	90V, 3.0 ohm

FEATURES

- Gate Oxide Breakdown, ±40V min
- Low Output and Transfer Capacitances
- Extended Safe Operating Area
- Complementary P-Channel Devices Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Drain-Source Voltage
- VN0104 ..... +40V
- VN0106 ..... +60V
- VN0109 ..... +90V

Drain-Gate Voltage (V_{GS} = 0)
- VN0104 ..... +40V
- VN0106 ..... +60V
- VN0109 ..... +90V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_A = +25°C	T_C = +25°C
TO-92(N3)pkg.	.23A	.42A

Peak Pulsed Drain Current ..... +2.0A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C
TO-92(N3)pkg.	0.30W	1.0W

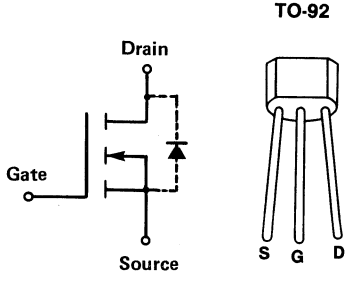
Linear Derating Factor

	T_A = +25°C	T_C = +25°C
TO-92(N3)pkg.	3.0mW/°C	10mW/°C

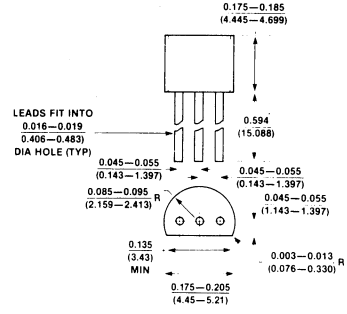
Operating Junction and Storage Temperature Range ..... -55°C to +150°C

Lead Temperature (1/16" from mounting surface for 30 sec.) ..... +260°C

PIN CONFIGURATION

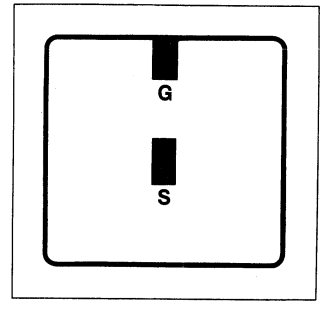


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .0445 x .0460 x .013 inches
Drain is backside contact.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

#	PARAMETER	VN0104 MIN	VN0104 TYP	VN0104 MAX	VN0106 MIN	VN0106 TYP	VN0106 MAX	VN0109 MIN	VN0109 TYP	VN0109 MAX	UNIT	TEST CONDITIONS		
1	BV_{DSS} Drain-Source Breakdown Voltage	40	60		60	90		90	105		V	I_D = 1.0mA, V_{GS} = 0		
2	I_{DSS} Drain-Source Off Leakage Current			100							μA	V_{DS} = 32V	T_A = +125°C	
3							100					V_{DS} = 48V		
4										100		V_{DS} = 72V	V_{GS} = 0	
5			.01	1.0								V_{DS} = 40V		
6						.01	1.0					V_{DS} = 60V	V_{GS} = 0	
7									.01	1.0		V_{DS} = 90V		
8	I_{GBS} Gate-Body Leakage Current			±1.0			±1.0			±1.0	μA	V_{GB} = ±40V	V_{DS} = 0	
9				±10			±10			±10	nA	V_{GB} = ±20V		
10	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.8		2.4	0.8		2.4	0.8		2.4	V	V_{DS} = V_{GS}, I_D = 1.0mA		
11	$r_{DS(on)}$ Drain-Source On Resistance			5.0			5.0			5.0	ohms	V_{GS} = 5V, I_D = .25A		(Note 1)
12				3.0			3.0			3.0		V_{GS} = 10V, I_D = 1.0A		
13	$I_{D(on)}$ On Drain Current	.75			.75			.75			A	V_{GS} = 5V	V_{DS} = 25V	
14		2.0			2.0			2.0				V_{GS} = 10V		
15	g_{fs} Common-Source Forward Transcond.	300			300			300			mmhos	V_{DS} = 25V, I_D = 0.5A f = 1KHz		
16	V_{SD} Source-Drain Forward Voltage			1.8			1.8			1.8	V	I_{SD} = 1.0A, V_{GS} = 0		
17	c_{iss} Common-Source Input Capacitance			60			60			60	pF	V_{DS} = 25V V_{GS} = 0 f = 1MHz		
18	c_{oss} Common-Source Output Capacitance		11	25		11	25		11	25				
19	c_{rss} Common-Source Reverse Transfer Capacitance		1.5	5.0		1.5	5.0		1.5	5.0				
20	t_{on} Turn ON Time		8.0	13		8.0	13		8.0	13	nS	V_{DD} = 25V, $V_{G(on)}$ = 10V R_G = 51Ω, R_L = 25Ω		
21	t_{off} Turn OFF Time		8.0	17		8.0	17		8.0	17				

NOTE 1: Pulse Test, 80μSec, 1% Duty Cycle

TOPAZ SEMICONDUCTOR

VN0610LL, VN2222LL

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- High Gate Oxide Breakdown, ±40V min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +60V

Drain-Gate Voltage (V_{GS}= 0) ..... +60V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_A = 25°C	T_C = 25°C
VN0610LL	.18A	.32A
VN2222LL	.15A	.26A

Peak Pulsed Drain Current 1.0A

Continuous Device Dissipation

T_A = +25°C	T_C = +25°C	
0.30	1.0	W

Linear Derating Factor

T_A = +25°C	T_C = +25°C	
2.4	8.0	mW/°C

Operating Junction Temperature Range ..... -55 to +150°C

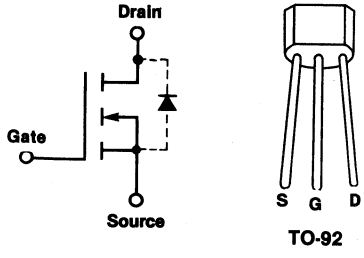
Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

ORDERING INFORMATION

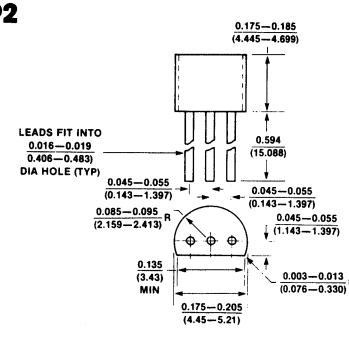
TO-92 Plastic Package	VN0610LL	VN2222LL
Description	60V, 5 ohm	60V, 7.5 ohm

SCHEMATIC DIAGRAM/PACKAGE



TO-92

PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTICS		VN0610LL			VN2222LL			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60	100		60	100		V	I_D = 100μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8	1.9	2.5	0.6	1.9	2.5	V	I_D = 1.0mA, V_{DS} = V_{GS}
3		I_{GBS}	Gate-Body Leakage Current		±1.0	±100		±1.0	±100	nA	V_{GS} = ±30V, V_{DS} = 0
4		I_{DSS}	Drain-Source OFF Leakage Current		0.1	10		0.1	10	μA	V_{DS} = 48V, V_{GS} = 0
5					5.0	500		5.0	500		T_A = +125°C
6		$I_{D(on)}$	ON Drain Current	1.0	2.2		1.0	2.2		A	V_{DS} = 10V, V_{GS} = 10V (Note 1)
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.9	1.5		0.9	1.5	V	V_{GS} = 5V, I_D = 0.2A (Note 1)
8					1.5	2.5		1.5	3.75		V_{GS} = 10V, I_D = 0.5A (Note 1)
9		$r_{DS(on)}$	Drain-Source ON Resistance		4.5	7.5		4.5	7.5	ohms	V_{GS} = 5V, I_D = 0.2A (Note 1)
10					3.0	5.0		3.0	7.5		V_{GS} = 10V, I_D = 0.5A (Note 1)
11					4.7	9.0		4.7	13.5		T_A = +125°C
12	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	100	400		100	400		mmhos	V_{DS} = 10V, I_D = 0.5A f = 1KHz (Note 1)
13		C_{iss}	Common-Source Input Capacitance		80	100		80	100	pF	V_{DS} = 15V, V_{GS} = 0 f = 1MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		1.3	5.0		1.3	5.0		
15		C_{OSS}	Common-Source Output Capacitance		10.5	25		10.5	25		
16		t_{on}	Turn-On Time		5.0	10		5.0	10	nSec	V_{DD} = 15V, $V_{G(on)}$ = 10V
17		t_{off}	Turn-Off Time		6.0	10		6.0	10		R_G = 25Ω, R_L = 25Ω

Note 1: Pulse Test 80μ Sec, 1% Duty Cycle

TOPAZ SEMICONDUCTOR

VN10KN

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- High Gate Oxide Breakdown, ±30V min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +60V

Drain-Gate Voltage (V_{GS}= 0) ..... +60V

Gate-Source Voltage ..... ±30V

Continuous Drain Current

T_A = 25°C	T_C = 25°C
.24A	.32A

Peak Pulsed Drain Current 1.0A

Continuous Device Dissipation

T_A = +25°C	T_C = +25°C	
0.30	1.0	W

Linear Derating Factor

T_A = +25°C	T_C = +25°C	
2.4	8.0	mW/°C

Operating Junction Temperature Range ..... -55 to +150°C

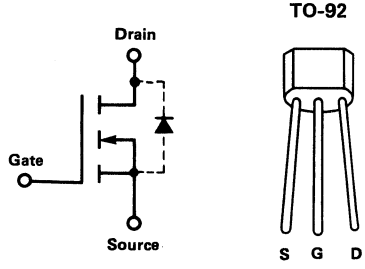
Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

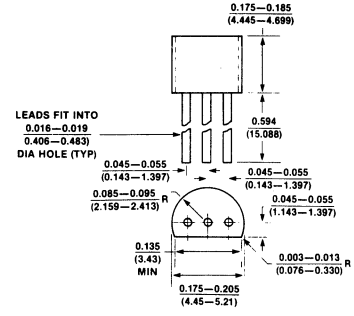
ORDERING INFORMATION

TO-92 Plastic Package	VN10KN3
Description	60V, 5 ohm

SCHEMATIC DIAGRAM/PACKAGE



PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		VN10KN MIN	VN10KN TYP	VN10KN MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60	100		V	I_D = 100μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8	1.9	2.5	V	I_D = 1.0mA, V_{DS} = V_{GS}
3	STATIC	I_{GBS}	Gate-Body Leakage Current		±1.0	±100	nA	V_{GS} = ±15V, V_{DS} = 0
4	STATIC	I_{DSS}	Drain-Source OFF		0.1	10	μA	V_{DS} = 40V, V_{GS} = 0
5	STATIC		Leakage Current		5.0	500		T_A = 125°C
6	STATIC	$I_{D(on)}$	ON Drain Current	0.25			A	V_{GS} = 5V, V_{DS} = 10V (Note 1)
7	STATIC			0.75				V_{GS} = 10V
8	STATIC	$V_{DS(on)}$	Drain-Source ON Voltage		1.5	2.5	V	V_{GS} = 10V, I_D = 0.5A (Note 1)
9	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		3.0	5.0	ohms	V_{GS} = 10V, I_D = 0.5A (Note 1)
10	STATIC				4.7	9.0		T_A = +125°C
11	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	100	400		mmhos	V_{DS} = 10V, I_D = 0.5A f = 1KHz (Note 1)
12	DYNAMIC	C_{iss}	Common-Source Input Capacitance		80	100	pF	V_{DS} = 15V, V_{GS} = 0 f = 1MHz
13	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.3	5.0		
14	DYNAMIC	C_{OSS}	Common-Source Output Capacitance		10.5	25		
15	DYNAMIC	t_{on}	Turn-On Time		5.0	10	nSec	V_{DD} = $V_{G(on)}$ = 10V
16	DYNAMIC	t_{off}	Turn-Off Time		6.0	10		R_G = 25Ω, R_L = 25Ω

Note 1: Pulse Test 80μ Sec, 1% Duty Cycle

TOPAZ SEMICONDUCTOR

VN10LM, VN2222LM

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

FEATURES

- High Gate Oxide Breakdown, ±40V min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Drain-Source Voltage ..... +60V

Drain-Gate Voltage (V_{GS}= 0) ..... +60V

Gate-Source Voltage ..... ±40

Continuous Drain Current

	T_A = 25°C	T_C = 25°C
VN10LM	.19A	.44A
VN2222LM	.16A	.36A

Peak Pulsed Drain Current 1.0A

Continuous Device Dissipation

T_A = +25°C	T_C = +25°C	
0.36	1.8	W

Linear Derating Factor

T_A = +25°C	T_C = +25°C	
2.9	14.4	mW/°C

Operating Junction Temperature Range ..... -55 to +150°C

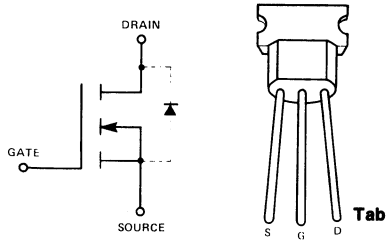
Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

ORDERING INFORMATION

TO-237 Plastic Package	VN10LM	VN2222LM
Description	60V, 5 ohm	60V, 7.5 ohm

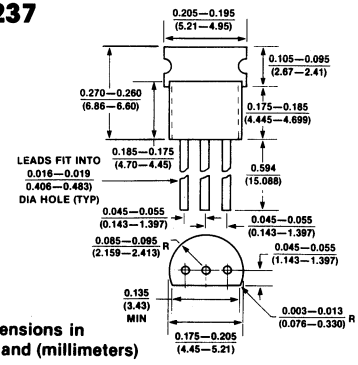
SCHEMATIC DIAGRAM/PACKAGE



TO-237

PACKAGE DIMENSIONS

TO-237



All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		VN10LM			VN2222LM			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60	100		60	100		V	I_D=100μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate-Source	0.8	1.9	2.5	0.6	1.9	2.5	V	I_D = 1.0mA, V_{DS} = V_{GS}
3		I_{GBS}	Gate-Body Leakage Current		±1.0	±100		±1.0	±100	nA	V_{GS} = ±30V, V_{DS} = 0
4		I_{DSS}	Drain-Source OFF Leakage Current		0.1	10		0.1	10	μA	V_{DS} = 48V, V_{GS} = 0
5					5.0	500		5.0	500		T_A = 125°C
6		$I_{D(on)}$	ON Drain Current	1.0	2.2		1.0	2.2		A	V_{DS} = 10V, V_{GS} = 10V (Note 1)
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.9	1.5		0.9	1.5	V	V_{GS} = 5V, I_D = 0.2A (Note 1)
8					1.5	2.5		1.5	3.75		V_{GS} = 10V, I_D = 0.5A (Note 1)
9		$r_{DS(on)}$	Drain-Source ON Resistance		4.5	7.5		4.5	7.5	ohms	V_{GS} = 5V, I_D = 0.2A (Note 1)
10					3.0	5.0		3.0	7.5		V_{GS} = 10V, I_D = 0.5A (Note 1)
11					4.7	9.0		4.7	13.5		T_A = +125°C
12	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	100	400		100	400		mmhos	V_{DS} = 10V, I_D = 0.5A f = 1KHz (Note 1)
13		C_{iss}	Common-Source Input Capacitance		80	100		80	100	pF	V_{DS} = 15V, V_{GS} = 0 f = 1MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		1.3	5.0		1.3	5.0		
15		C_{oss}	Common-Source Output Capacitance		10.5	25		10.5	25		
16		t_{on}	Turn-On Time		5.0	10		5.0	10	nSec	V_{DD} = 15V, $V_{G(on)}$ = 10V
17		t_{off}	Turn-Off Time		6.0	10		6.0	10		R_G = 25Ω, R_L = 25Ω

Note 1: Pulse Test 80μ Sec, 1% Duty Cycle

TOPAZ SEMICONDUCTOR

VN2410

N-CHANNEL ENHANCEMENT-MODE D-MOS FET

ORDERING INFORMATION

Sorted Chips in Waffle Pack	VN2410CHP
TO-92 Plastic Package	VN2410L
Description	240V, 10 ohm

FEATURES

- Gate Stand-off Voltage, ±40V min.

APPLICATIONS

- Motor Controls
- Line Drivers
- Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Drain-Source Voltage 240V
Drain-Gate Voltage (R_{GS} = 1MΩ) 240V
Gate-Source Voltage ..... ±40V
Continuous Drain Current

	T_C = +100°C	T_C = +25°C
VN2410L	0.14	0.22A

Peak Pulsed Drain Current 1.0A

Maximum Power Dissipation

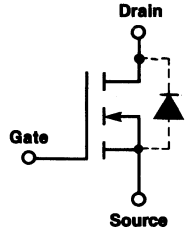
	T_C = +100°C	T_C = +25°C
VN2410L	0.4W	3.0W

Linear Derating Factor

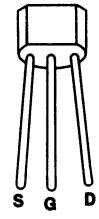
	Junction to Ambient (mW/°C)	Junction to Case (mW/°C)
VN2410L	3.0	24

Operating Junction and Storage Temperature Range ..... -55 to +150°C
Lead Temperature (1/16" from mounting surface for 10 Sec) ..... +260°C

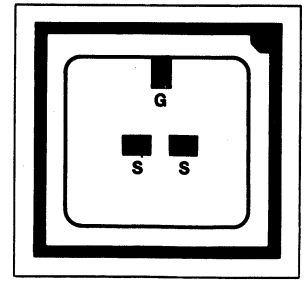
PIN CONFIGURATION



TO-92



CHIP CONFIGURATION



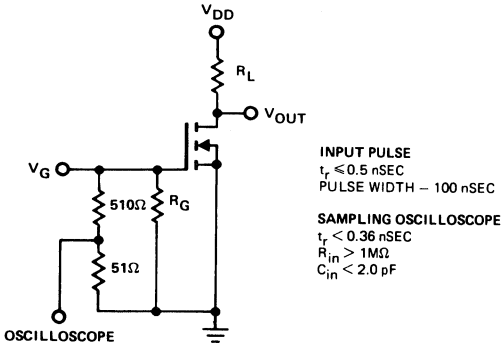
Dimensions: 0.054 x 0.056 x 0.013 inches
Drain is backside contact.

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

#		CHARACTERISTIC		VN2410 MIN	VN2410 TYP	VN2410 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	240	290		V	I_D = 250μA, V_{GS} = 0	
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	1.0	1.3	2.0	V	V_{DS} = V_{GS}	
3				0.4				I_D = 1 mA	T_C = +125°C
4		I_{GBS}	Gate-Body Leakage Current			100	nA	V_{GS} = 15V, V_{DS} = 0	
5						500			T_C = +125°C
6						-100		V_{GS} = -15V, V_{DS} = 0	
7		I_{DSS}	Drain-Source OFF Leakage Current			10	μA	V_{DS} = 120V	
8						500		V_{GS} = 0	T_C = +125°C
9		$I_{D(on)}$	ON Drain Current(1)	1.0	1.3		A	V_{DS} = 25V, V_{GS} = 10V	
10		$V_{DS(on)}$	Drain-Source(1) ON Voltage		0.7	1.0	V	V_{GS} = 2.5V, I_D = 0.1A	
11					3.9	5.0		V_{GS} = 10V, I_D = 0.5A	
12		$r_{DS(on)}$	Drain-Source(1) ON Resistance		7.8	10	ohms	V_{GS} = 10V	
13						24.7		I_D = 0.5A	T_C = +125°C
14					7.0	10		V_{GS} = 2.5V, I_D = 0.1A	
15	DYNAMIC	g_{fs}	Common-Source(1) Forward Transcond.	0.3	0.75		S	V_{DS} = 25V, I_D = 0.5A, f = 1KHz	
16		C_{iss}	Common-Source Input Capacitance			125	pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	
17		C_{rss}	Common-Source Reverse Transfer Capacitance		6.0	20			
18		C_{OSS}	Common-Source Output Capacitance		15	50			
19		$t_{d(on)}$	Turn-ON Delay Time			8.0	nsec	V_{DD} = 60V R_L = 600 ohms R_G = 25 ohms $V_{G(on)}$ = 10V	
20		t_r	Rise Time			8.0			
21		$t_{d(off)}$	Turn-OFF Delay Time			23			
22		t_f	Fall Time			24			
23	DIODE	I_S	Continuous Source Current	.14			A		
24		I_{SM}	Peak Source Current(1)	1.0					
25		V_{SD}	Source-Drain(1) Forward Voltage		-1.2		V	V_{GS} = 0, I_S = -0.14A	

Note 1: Pulse test 80μSec, 1% Duty Cycle

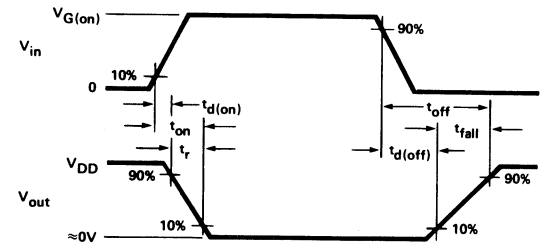
SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

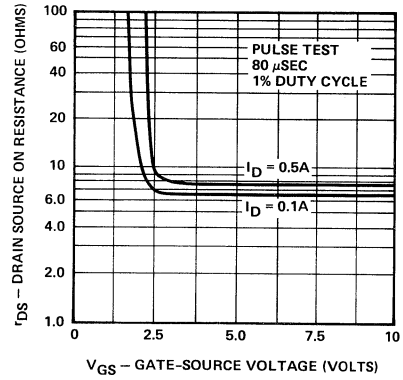
SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1M\Omega$
$C_{in} < 2.0$ pF

TEST WAVEFORMS

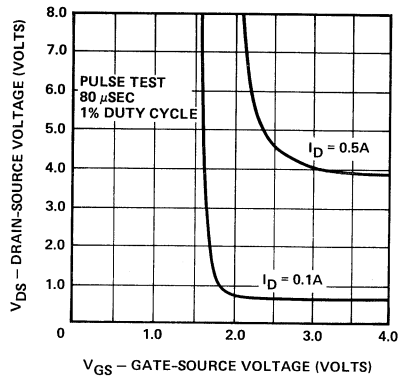


TYPICAL PERFORMANCE CHARACTERISTICS (T_C = +25°C unless otherwise noted)

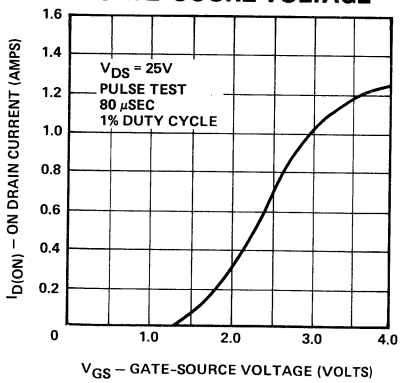
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



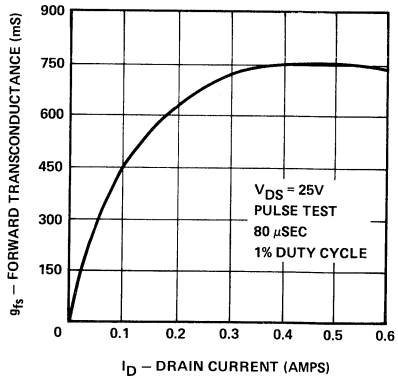
ON VOLTAGE CHARACTERISTICS



ON DRAIN CURRENT —vs— GATE-SOURE VOLTAGE



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

VP0104, VP0106 VP0109

P-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

TO-92 Plastic Package	VP0104N3	VP0106N3	VP0109N3
Sorted Chips in Carriers	VP0104ND	VP0106ND	VP0109ND
Description	-40V, 8.0 ohm	-60V, 8.0 ohm	-90V, 8.0 ohm

FEATURES

- Gate Oxide Breakdown, ±40V min
- Low Output and Transfer Capacitances
- Extended Safe Operating Area
- Complementary N-Channel Devices Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Drain-Source Voltage
- VP0104 ..... -40V
- VP0106 ..... -60V
- VP0109 ..... -90V

Drain-Gate Voltage (V_{GS} = 0)
- VP0104 ..... -40V
- VP0106 ..... -60V
- VP0109 ..... -90V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_A = +25°C	T_C = +25°C
TO-92(N3)pkg.	-.14A	-.26A

Peak Pulsed Drain Current ..... -0.5A

Continuous Device Dissipation

	T_A = +25°C	T_C = +25°C
TO-92(N3)pkg.	0.30W	1.0W

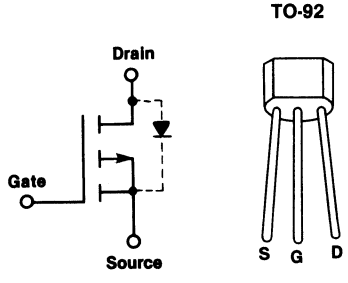
Linear Derating Factor

	T_A = +25°C	T_C = +25°C
TO-92(N3)pkg.	3.0mW/°C	10mW/°C

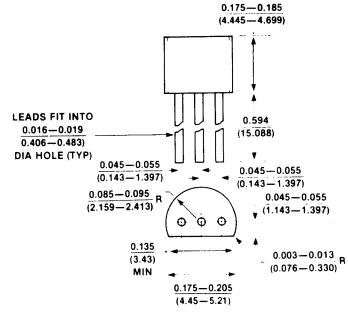
Operating Junction and Storage Temperature Range ..... -55°C to +150°C

Lead Temperature (1/16" from mounting surface for 30 sec.) ..... +260°C

PIN CONFIGURATION

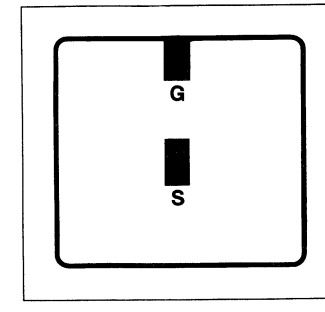


PACKAGE DIMENSIONS TO-92



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



Dimensions: .0445 x .0460 x .013 inches
Drain is backside contact.

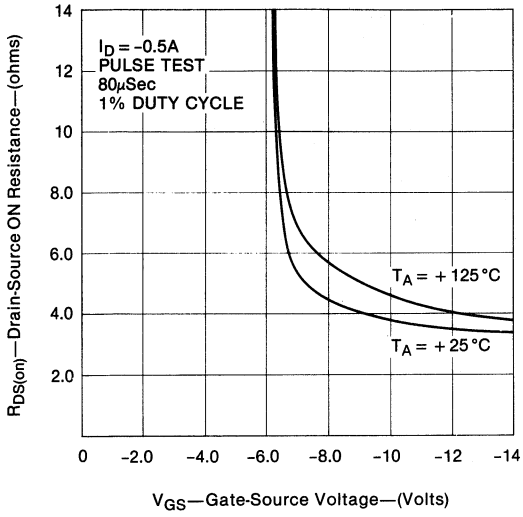
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

#	PARAMETER	VP0104 MIN	VP0104 TYP	VP0104 MAX	VP0106 MIN	VP0106 TYP	VP0106 MAX	VP0109 MIN	VP0109 TYP	VP0109 MAX	UNIT	CONDITIONS
1	BV_{DSS} Drain-Source Breakdown Voltage	-40	-60		-60	-90		-90	-105		V	I_D = -1.0mA, V_{GS} = 0
2	I_{DSS} Drain-Source Off Leakage Current			-1.0							mA	V_{DS} = -32V, T_A = +125°C
3							-1.0					V_{DS} = -48V
4										-1.0		V_{DS} = -72V, V_{GS} = 0
5			-.01	-10							µA	V_{DS} = -40V
6						-.01	-10					V_{DS} = -60V, V_{GS} = 0
7									-.01	-10		V_{DS} = -90V
8	I_{GBS} Gate-Body Leakage Current			±1.0			±1.0			±1.0	µA	V_{GB} = ±40V, V_{DS} = 0
9				±10			±10			±10	nA	V_{GB} = ±20V
10	$V_{GS(th)}$ Gate-Source Threshold Voltage	-1.5		-3.5	-1.5		-3.5	-1.5		-3.5	V	V_{DS} = V_{GS}, I_D = -1.0mA
11	$r_{DS(on)}$ Drain-Source On Resistance		10	15		10	15		10	15	ohms	V_{GS} = -5V, I_D = -0.1A
12			4.0	8.0		4.0	8.0		4.0	8.0		V_{GS} = -10V, I_D = -0.5A
13	$I_{D(on)}$ On Drain Current	-0.1	-0.2		-0.1	-0.2		-0.1	-0.2		A	V_{GS} = -5V, V_{DS} = -25V (Note 1)
14		-0.5	-1.2		-0.5	-1.2		-0.5	-1.2			V_{GS} = -10V
15	g_{fs} Common-Source Forward Transcond.	150	275		150	275		150	275		mmhos	V_{DS} = -25V, I_D = -0.5A, f = 1KHz
16	V_{SD} Source-Drain Forward Voltage			-2.0			-2.0			-2.0	V	I_{SD} = -1.0A, V_{GS} = 0
17	C_{iss} Common-Source Input Capacitance			60			60			60	pF	V_{DS} = -25V, V_{GS} = 0, f = 1MHz
18	C_{oss} Common-Source Output Capacitance		11	30		11	30		11	30		
19	C_{rss} Common-Source Reverse Transfer Capacitance		1.5	8.0		1.5	8.0		1.5	8.0		
20	t_{on} Turn ON Time		8.0	16		8.0	16		8.0	16	nS	V_{DD} = -25V, $V_{G(on)}$ = -10V
21	t_{off} Turn OFF Time		8.0	15		8.0	15		8.0	15		R_G = 51Ω, R_L = 51Ω

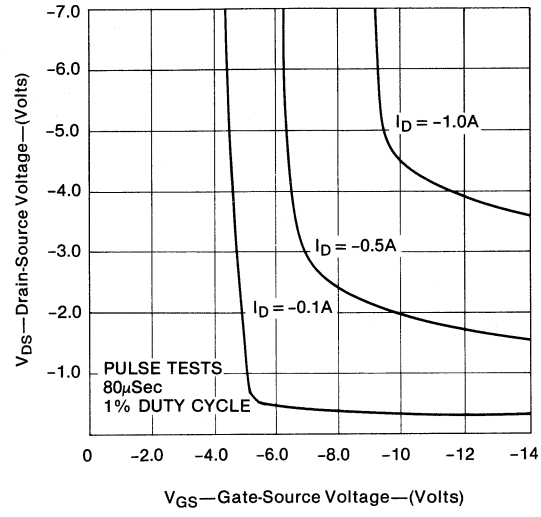
NOTE 1: Pulse Test, 80µSec, 1% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

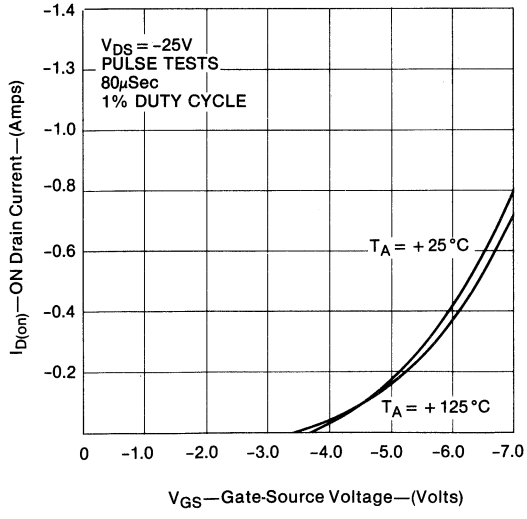
DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE



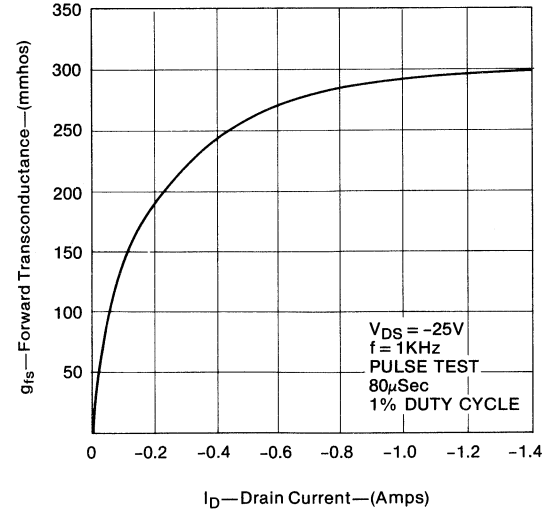
ON VOLTAGE CHARACTERISTICS



ON DRAIN CURRENT
—VS—
GATE SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



TOPAZ SEMICONDUCTOR

VP0808, VP1008

P-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Waffle Pack	VP0808CHP	VP1008CHP
TO-92 Plastic Package	VP0808L	VP1008L
TO-237 Plastic Package	VP0808M	VP1008M
Description	-80V, 5.0 ohm	-100V, 5.0 ohm

FEATURES

- Gate Stand-off Voltage, ±40V min.
- Low Output and Transfer Capacitances
- N-Channel Complements Available

APPLICATIONS

- Motor Controls
- Logic Interfaces
- Pulse Amplifiers

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Drain-Source Voltage
- VP1008 ..... -100V
- VP0808 ..... -80V

Drain-Gate Voltage (R_{GS} = 1MΩ)
- VP1008 ..... -100V
- VP0808 ..... -80V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_C = +100°C	T_C = +25°C
TO-92 Pkg.	-.13A	-.21A
TO-237 Pkg.	-.21A	-.33A

Peak Pulsed Drain Current ..... -3.0A

Maximum Power Dissipation

	T_C = +100°C	T_C = +25°C
TO-92 Pkg.	0.4W	3.0W
TO-237 Pkg.	1.0W	4.3W

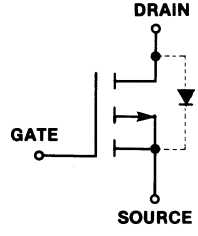
Linear Derating Factor

	Junction to Ambient (mW/°C)	Junction to Case (mW/°C)
TO-92 Pkg.	3.0	24
TO-237 Pkg.	8.0	34

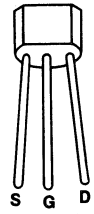
Operating Junction and Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 10 Sec) ..... +300°C

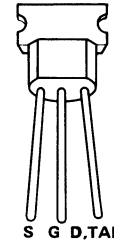
PIN CONFIGURATIONS



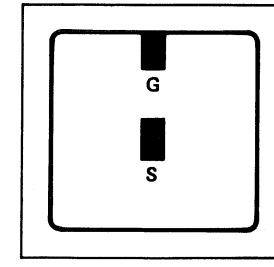
TO-92



TO-237



CHIP CONFIGURATION



Dimensions: 0.0445 x 0.0460 x 0.013 inches
Drain is backside contact.

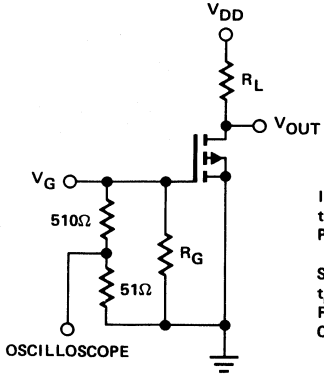
Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

#		CHARACTERISTIC		VP0808 MIN	VP0808 TYP	VP0808 MAX	VP1008 MIN	VP1008 TYP	VP1008 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-80			-100			V	I_D = -10μA, V_{GS} = 0	
2	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	-2.0		-4.5	-2.0		-4.5	V	V_{DS} = V_{GS} I_D = -1.0mA	
3	STATIC	I_{GBS}	Gate-Body Leakage Current			-100			-100	nA	V_{GS} = -30V, V_{DS} = 0	
4	STATIC	I_{GBS}	Gate-Body Leakage Current			100			100	nA	V_{GS} = +30V, V_{DS} = 0	
5	STATIC	I_{DSS}	Drain-Source OFF Leakage Current			-10				μA	V_{DS} = -80V	
6	STATIC	I_{DSS}	Drain-Source OFF Leakage Current			-500				μA	V_{GS} = 0	T_C = +125°C
7	STATIC	I_{DSS}	Drain-Source OFF Leakage Current						-10	μA	V_{DS} = -100V	
8	STATIC	I_{DSS}	Drain-Source OFF Leakage Current						-500	μA	V_{GS} = 0	T_C = +125°C
9	STATIC	$I_{D(on)}$	ON Drain Current[1]	-1.1			-1.1			A	V_{DS} = -25V, V_{GS} = -10V	
10	STATIC	$V_{DS(on)}$	Drain-Source[1] ON Voltage		-4.5	-5.0		-4.5	-5.0	V	V_{GS} = -10V, I_D = -1.0A	
11	STATIC	$r_{DS(on)}$	Drain-Source[1] ON Resistance		4.5	5.0		4.5	5.0	ohms	V_{GS} = -10V	
12	STATIC	$r_{DS(on)}$	Drain-Source[1] ON Resistance			8.0			8.0	ohms	I_D = -1.0A	T_C = +125°C
13	DYNAMIC	g_{fs}	Common-Source[1] Forward Transcond.	200	270		200	270		mS	V_{DS} = -25V, I_D = -0.5A, f = 1KHz	
14	DYNAMIC	C_{iss}	Common-Source Input Capacitance		60	150		60	150	pF	V_{DS} = -25V, V_{GS} = 0 f = 1MHz	
15	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		8.0	25		8.0	25	pF		
16	DYNAMIC	C_{OSS}	Common-Source Output Capacitance		11	60		11	60	pF		
17	DYNAMIC	$t_{d(on)}$	Turn-ON Delay Time			10			10	nsec	V_{DD} = -25V R_L = 45 ohms R_G = 25 ohms $V_{G(on)}$ = -10V	
18	DYNAMIC	t_r	Rise Time			15			15	nsec		
19	DYNAMIC	$t_{d(off)}$	Turn-OFF Delay Time			10			10	nsec		
20	DYNAMIC	t_f	Fall Time			15			15	nsec		
21	DIODE	I_S	Continuous Source Current	-.21			-.21			A	TO-92 Pkg.	
22	DIODE	I_S	Continuous Source Current	-.33			-.33			A	TO-237 Pkg.	
23	DIODE	I_{SM}	Peak Source Current[1]			-3.0			-3.0	A		
24	DIODE	V_{SD}	Source-Drain[1] Forward Voltage		1.2			1.2		V	V_{GS} = 0	I = .21A, TO-92 Pkg.
25	DIODE	V_{SD}	Source-Drain[1] Forward Voltage		1.2			1.2		V	V_{GS} = 0	I = .33A, TO-237 Pkg.

Note 1: Pulse Test 80μSec, 1% Duty Cycle

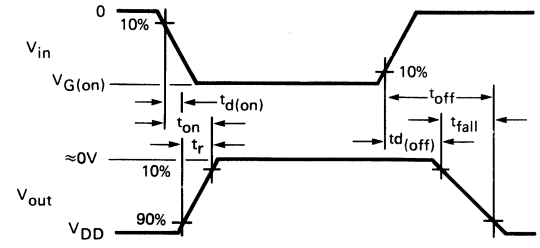
SWITCHING TIME TEST CIRCUIT



INPUT PULSE
$t_r \leq 0.5$ nSEC
PULSE WIDTH – 100 nSEC

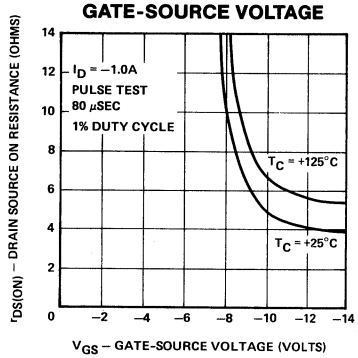
SAMPLING OSCILLOSCOPE
$t_r < 0.36$ nSEC
$R_{in} > 1$ MΩ
$C_{in} < 2.0$ pF

TEST WAVEFORMS

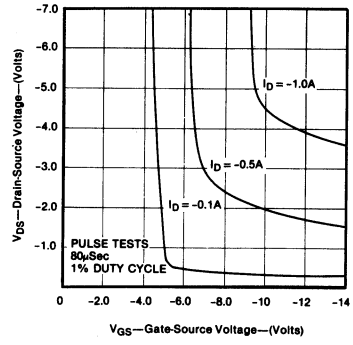


TYPICAL PERFORMANCE CHARACTERISTICS (T_C = +25°C unless otherwise specified)

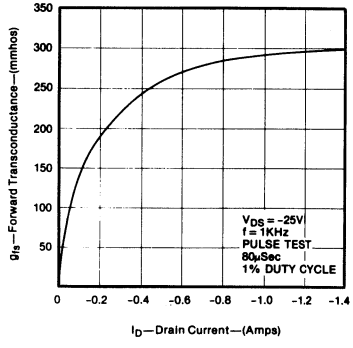
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



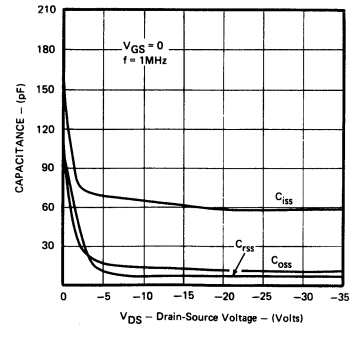
ON VOLTAGE CHARACTERISTICS



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



CAPACITANCES —vs— DRAIN-SOURCE VOLTAGE



TOPAZ SEMICONDUCTOR

VQ1000

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS POWER FET ARRAY

ORDERING INFORMATION

14 Pin Plastic DIP	VQ1000J
Description	60V, 5.5 ohms

FEATURES

- Inherent Current Sharing Capability when Paralleled
- Simple Straightforward DC Biasing
- Extended Safe Operating Area
- CMOS and TTL Compatible

APPLICATIONS

- High-Speed Pulse Amplifiers
- CMOS Logic to High-Current Interfaces
- High-Speed Switching
- Line Drivers
- Stepper Motor Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

Drain-Source Voltage 60V
Drain-Gate Voltage (V_{GS} = 0) 60V
Gate-Source Voltage ..... ± 40V
Continuous Drain Current

	T_A = 25°C	T_C = 25°C	
Total Package	.29	.51	A
Single Device	.20	.36	A

Peak Pulsed Drain Current 1.0A
Continuous Device Dissipation

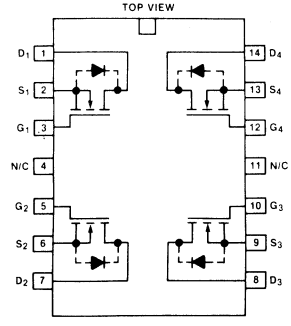
	T_A = +25°C	T_C = +25°C	
Total Package	.64	2.0	W
Single Device	.30	1.0	W

Linear Derating Factor

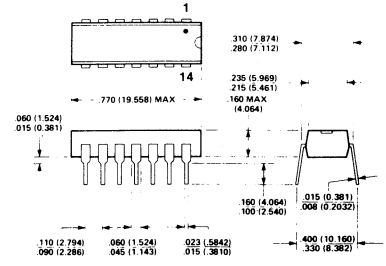
	T_A = +25°C	T_C = +25°C	
Total Package	5.1	16	mW/°C
Single Device	2.4	8.0	mW/°C

Operating Junction Temperature Range ..... -55 to +150°C
Storage Temperature Range ..... -55 to +150°C
Lead Temperature (1/16" from mounting surface for 30 Sec) ..... +260°C

SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS 14 PIN PLASTIC DIP



All dimensions in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

#		CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	60	105		V	I_D = 100μA, V_{GS} = 0	
2		$V_{GS(th)}$ Gate Source Threshold Voltage	0.8	1.9	2.5	V	$V_{DS} = V_{GS}$, I_D = 1.0mA	
3		I_{GBS} Gate-Body Leakage Current		.10	100	nA	V_{GS} = 10V	
4				10	500		V_{DS} = 0	T_A = +125°C
5				-.10	-100		V_{GS} = -10V, V_{DS} = 0	
6		I_{DSS} Drain-Source OFF Leakage Current		.10	10	μA	V_{DS} = 60V	
7				10	500		V_{GS} = 0	T_A = +125°C
8		$I_{D(on)}$ Drain-Source ON Current (Note 1)	0.2	1.3		A	V_{DS} = 10V	V_{GS} = 5V
9			0.5	2.5				V_{GS} = 10V
10		$V_{DS(on)}$ Drain-Source ON Voltage (Note 1)			1.50	V	V_{GS} = 5V, I_D = 0.2A	
11					1.65		V_{GS} = 10V, I_D = 0.3A	
12		$r_{DS(on)}$ Drain-Source ON Resistance (Note 1)			7.5	ohms	V_{GS} = 5V, I_D = 0.2A	
13					5.5		V_{GS} = 10V I_D = 0.3A	
14					7.6			T_A = +125°C
15	DYNAMIC	g_{fs} Common-Source Forward Transcond (Note 1)	100	400		mmhos	V_{DS} = 10V, I_D = 0.5A f = 1KHz	
16		C_{iss} Common-Source Input Capacitance			60	pF	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	
17		C_{rss} Common-Source Reverse Transfer Capacitance			5.0			
18		C_{oss} Common-Source Output Capacitance			25			
19		t_{on} Turn-ON Time			10	nS	V_{DD} = 15V, $V_{G(on)}$10V	
20		t_{off} Turn-OFF Time			10		R_G = 25Ω, R_L = 25Ω	

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SECTION 3

ANALOG SWITCHES

TYPE NO.	TEMP. RANGE	PACKAGE	CONFIG.	LOGIC '0'	LOGIC LEVELS (VOLTS)	$r_{DS(ON)}$ TYP. (OHMS)	OFF(1) ISOLATION (dB)	ANALOG RANGE (VOLTS)	SWITCH BANDWIDTH (MHz)
CDG201AK	MIL	16-CDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG201BJ	IND	16-PDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG201BK	IND	16-CDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG201CJ	COMM	16-PDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG211CJ	COMM	16-PDIP	4xSPST	ON	0.8-2.4	45	66	+10,-10	100
CDG308AK	MIL	16-CDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG308BJ	IND	16-PDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG308BK	IND	16-CDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG308CJ	COMM	16-PDIP	4xSPST	OFF	1.0-4.5	45	62	+10,-10	100
CDG309AK	MIL	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG309BJ	IND	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG309BK	IND	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG309CJ	COMM	16-CDIP	4xSPST	ON	1.0-4.5	45	62	+10,-10	100
CDG2214BJ	IND	8-PDIP	1xSPST	ON	1.0-4.5	45	82	+10,-10	250
CDG4308BJ	IND	20-PDIP	4xSPST	OFF	1.0-4.5	45	68	+10,-10	100
CDG4309BJ	IND	20-PDIP	4xSPST	ON	1.0-4.5	45	68	+10,-10	100
CDG5341AK	MIL	14-CDIP	DUAL T	OFF	1.0-4.5	110	80	+10,-10	50
CDG5341BJ	IND	14-PDIP	DUAL T	OFF	1.0-4.5	110	80	+10,-10	50
CDG5341BK	IND	14-CDIP	DUAL T	OFF	1.0-4.5	110	80	+10,-10	50
CDG5341CJ	COMM	14-PDIP	DUAL T	OFF	1.0-4.5	110	80	+10,-10	50

Note 1: R_L = 50 ohms, f = 10MHz

ANALOG MULTIPLEXERS

TYPE NO.	TEMP. RANGE	PACKAGE	CONFIG.	LOGIC LEVELS (VOLTS)	$r_{DS(ON)}$ TYP. (OHMS)	CROSS(1)(2) TALK (dB)	ANALOG RANGE (VOLTS)	SWITCH BANDWIDTH (MHz)
CDG4500AK	MIL	14-CDIP	4-CHANNEL	1.0-4.5	40	62	+10,-10	100
CDG4500BJ	IND	14-PDIP	4-CHANNEL	1.0-4.5	40	62	+10,-10	100
CDG4500BK	IND	14-CDIP	4-CHANNEL	1.0-4.5	40	62	+10,-10	100
CDG4500CJ	COMM	14-PDIP	4-CHANNEL	1.0-4.5	40	62	+10,-10	100

Note 1: R_L = 50 ohms, f = 10MHz

Note 2: All Channels, single Channel 80dB

8-BIT DIGITAL CONTROLLED ATTENUATOR

TYPE NO.	LOGIC LEVELS (VOLTS)	PACKAGE	ATTENUATION RANGE (dB)	ATTENUATION STEPS (dB)	ANALOG INPUT (VOLTS)
CDG4469J	1.0-4.5	Special, 16-Pin Ceramic	0 to 127.5	0.5	+9.0,-9.0

TYPE NO.	SOURCE	CONFIGURATION	PACKAGE	TOPAZ TYPE NO.
ADG201ABQ	1	4 x SPST	16-CDIP	CDG201BK
ADG201AKN	1	4 x SPST	16-PDIP	CDG201CJ
ADG201ATQ	1	4 x SPST	16-CDIP	CDG201AK
DG201A Series	6	4 x SPST		CDG201 Series
DG201AAK	10	4 x SPST	16-CDIP	CDG201AK
DG201ABK	10	4 x SPST	16-CDIP	CDG201BK
DG201ACJ	10	4 x SPST	16-PDIP	CDG201CJ
DG201ACK	10	4 x SPST	16-CDIP	CDG201BK
DG211	6	4 x SPST		CDG211CJ
DG211CJ	10	4 x SPST	16-PDIP	CDG211CJ
DG271BK	10	4 x SPST	16-CDIP	CDG201BK
DG271CJ	10	4 x SPST	16-PDIP	CDG201CJ
DG271CK	10	4 x SPST	16-CDIP	CDG201BK
DG308AAK	10	4 x SPST	16-CDIP	CDG308AK
DG308ABK	10	4 x SPST	16-CDIP	CDG308BK
DG308ACJ	10	4 x SPST	16-PDIP	CDG308CJ
DG308ACK	10	4 x SPST	16-CDIP	CDG308BK
DG309AK	10	4 x SPST	16-CDIP	CDG309AK
DG309BK	10	4 x SPST	16-CDIP	CDG309BK
DG309CJ	10	4 x SPST	16-PDIP	CDG309CJ
DG309CK	10	4 x SPST	16-CDIP	CDG309BK
DGP201AAK	10	4 x SPST	16-CDIP	CONTACT FACTORY
DGP201ABK	10	4 x SPST	16-CDIP	CONTACT FACTORY
DGP201ACJ	10	4 x SPST	16-PDIP	CONTACT FACTORY
HT201-2 Series	4	4 x SPST		CDG201 Series
HI201-5 Series	4	4 x SPST		CDG201 Series
HI201-2 Series	4	4 x SPST		CDG201 Series
HI201HS-5 Series	4	4 x SPST		CDG201 Series
IH5341 Series	6	2 x SPST DUAL T		CDG5341 Series
IH5341CPD	4	2 x SPST DUAL T	14-PDIP	CDG5341CJ
LF11201D	8	4 x SPST	16-CSB	CDG201AK
LF13201D	8	4 x SPST	16-CSB	CDG201BK
LF13201N	8	4 x SPST	16-PDIP	CDG201CJ
MP201DIAP	7	4 x SPST	16-CDIP	CDG201AK
MP201DIBP	7	4 x SPST	16-CDIP	CDG201BK
MP201DICJ	7	4 x SPST	16-PDIP	CDG201CJ
SW-201F Series	9	4 x SPST		CDG201 Series
SW-201G Series	9	4 x SPST		CDG201 Series

SOURCE

1—Analog Devices
3—Harris Semiconductor
4—GE/Intersil
6—Maxim
7—Micropower
8—National Semiconductor
9—Precision Monolithics
10—Siliconix

TOPAZ SEMICONDUCTOR

CDG201

QUAD MONOLITHIC SPST CMOS/D-MOS ANALOG SWITCH

ORDERING INFORMATION

Quad SPST, Logic '0' ON Break-Before-Make	16-Pin Plastic DIP	16-Pin Ceramic DIP
Commercial Temp. Range	CDG201CJ	—
Industrial Temp. Range	CDG201BJ	CDG201BK
Military Temp. Range	—	CDG201AK

FEATURES

- High OFF Isolation, 66 dB @ 10MHz
- Wide Bandwidth Switches, 0.9 x DC @ 100MHz
- Low Channel-to-Channel Crosstalk, -80 dB @ 10MHz
- TTL Compatible
- Industry Standard Pin-Out

APPLICATIONS

- Glitch-Free Analog Switches
- RF & Video Switches
- Track and Hold Switches
- Sample and Hold Switches

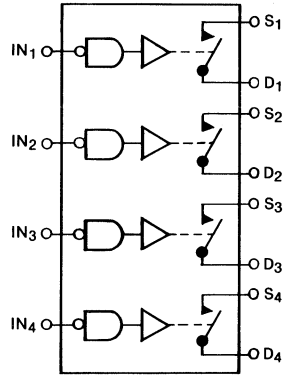
DESCRIPTION

The Topaz Semiconductor CDG201 Analog Switch features TTL compatible input logic and wide-band Lateral D-MOS switches on a single chip. The on-chip reference used for TTL compatibility gives the added advantage of constant logic switching over a wide range of supply voltages and temperature without a separate power supply. Industry standard pin-out makes the CDG201 particularly suitable for replacement of existing analog switches and at the same time upgrading high frequency performance.

NOTE

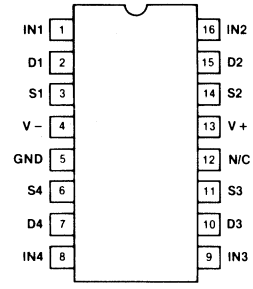
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (V_{DD} or GND).

FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches per Package
Switches shown in Logic "1" Input Position

PIN CONFIGURATION



TOP VIEW

LOGIC TABLE

Logic	Switch
0	ON
1	OFF

Logic '0' ≦ 0.8V
Logic '1' ≧ 2.4V

ABSOLUTE MAXIMUM RATINGS

V- Negative Supply Voltage ..... -20V
V+ Positive Supply Voltage ..... +20V
V_{IN} Control Input Voltage Range ..... V+ +0.3V, V- -0.3V
I_L Continuous Current, any Pin Except S or D ..... 20 mA
I_S Continuous Current, S or D ..... 30 mA
I_S Peak Pulsed Current, S or D, 80μsec, 1%, Duty Cycle ..... 90 mA
T_J Junction Temperature Range ..... -55 to +125°C
T_S Storage Temperature Range ..... -55 to +125°C
P_D Power Dissipation (derate at 5.5mW/°C, above +85°C) ..... 500 mW

RECOMMENDED OPERATING CONDITIONS

V- Negative Supply Voltage ..... -8.0 to -15V
V+ Positive Supply Voltage ..... +8.0 to +15V
V_{IN} Control Input Voltage Range ..... 0 to +5V
T_{OP} Operating Temperature
(A Suffix) ..... -55 to +125°C
(B Suffix) ..... -25 to +85°C
(C Suffix) ..... 0 to +70°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V- = -15V, V+ = +15V per channel, unless otherwise noted)

#	SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V_{ANALOG}		Analog Signal Range	-10		+10	V	
2	$r_{DS(on)}$	STATIC	Switch ON Resistance		40	80	Ω	V_S = -10V, V_{IN} = 0
3					45	80		V_S = +2.0V, V_{IN} = 0
4					100	160		V_S = +10V, V_{IN} = 0
5	V_{IH}		High Level Input Voltage	2.4			V	
6	V_{IL}		Low Level Input Voltage			0.8		
7	I_{IN}		Logic Input Leakage Current		0.01	0.1	μA	V_{IN} = +2.4V
8					0.02	0.1		V_{IN} = +15V
9	$I_{D(OFF)}$		Switch OFF Leakage Current		0.2	5.0	nA	V_D = +10V, V_S = -10V, V_{IN} = +2.4V
10	$I_{S(OFF)}$				0.4	5.0		V_S = +10V, V_D = -10V, V_{IN} = +2.4V
11	I-		Negative Supply Quiescent Current		-0.3	-1.0	mA	V_{IN} = 0 or +2.4
12	I+		Positive Supply Quiescent Current		0.6	2.0		
13	t_{ON}	DYNAMIC	Switch Turn-On Time		400	600	nSec	See Switching Times Test Circuit
14	t_{OFF}		Switch Turn-OFF Time		70	300		
15	O_{IRR}		OFF Isolation, Rejection Ratio	60	66		dB	f = 10 MHz, R_L = 50Ω
16	C_{CRR}		Cross-Coupling Rejection Ratio		80			
17	C_d		Drain-Node Capacitance		0.3		pF	V_D = V_s = 0, f = 1MHz, V_{IN} = +2.4V
18	C_s		Source-Node Capacitance		3.0			

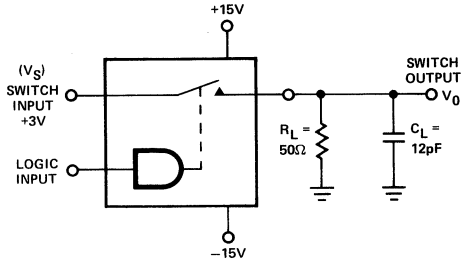
ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel unless otherwise noted)

LIMITS AT TEMPERATURE EXTREMES

#	SYMBOL		PARAMETER	MAXIMUM @ T_A = -55°C	-25°C	+70°C	+85°C	+125°C	UNITS	TEST CONDITIONS
1	V_{ANALOG}		Analog Signal Range	±10	±10	±10	±10	±10	V	
2	$r_{DS(on)}$	STATIC	Switch ON Resistance	80	80	120	120	150	Ω	V_S = -10V, V_{IN} = 0
3				80	80	120	120	150		V_S = +2.0V, V_{IN} = 0
4				160	160	240	240	300		V_S = +10V, V_{IN} = 0
5	I_{IN}		Logic Input Leakage Current	0.1	0.1	1.0	1.0	10	μA	V_{IN} = +2.4V
6				0.1	0.1	2.0	2.0	20		V_{IN} = +15V
7	$I_{D(OFF)}$		Switch OFF Leakage Current	5.0	5.0	100	100	1000	nA	V_D=+10V, V_S=-10V, V_{IN}= +2.4V
8	$I_{S(OFF)}$			5.0	5.0	100	100	1000		V_S=+10V, V_D=-10V, V_{IN}= +2.4V
9	I-		Supply Quiescent Currents	-1.0	-1.0	-1.0	-1.0	-1.0	mA	V_{IN} = 0 or +2.4V
10	I+			2.0	2.0	2.0	2.0	2.0		

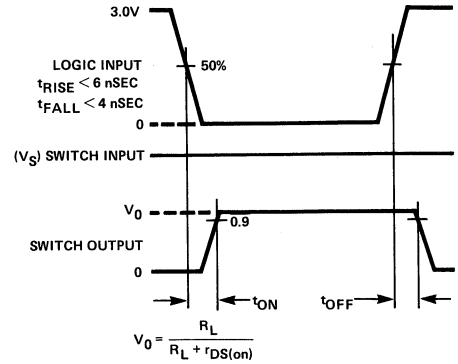
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

SWITCHING TIMES TEST CIRCUIT

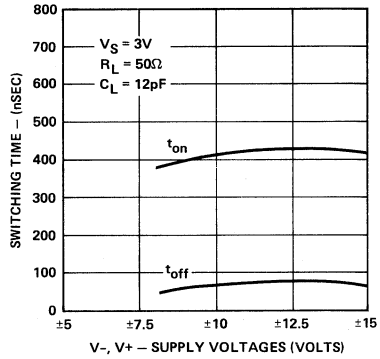


SWITCH ILLUSTRATED IN LOGIC "1", SWITCH OFF, POSITION

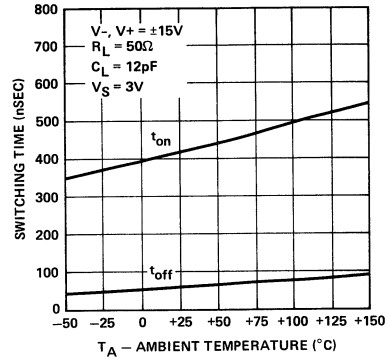
TEST WAVEFORMS



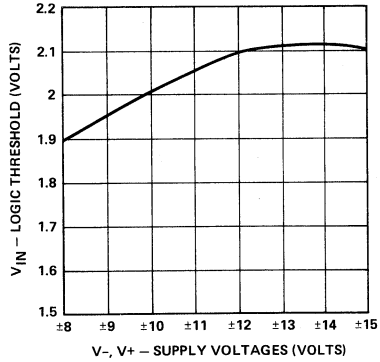
SWITCHING TIMES —VS— SUPPLY VOLTAGES



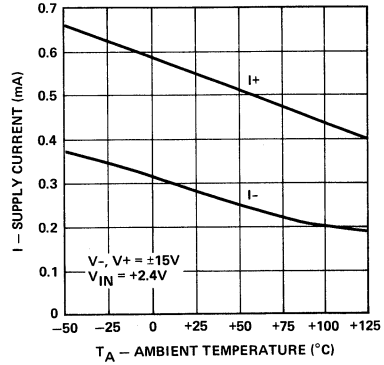
SWITCHING TIMES —VS— AMBIENT TEMPERATURE



LOGIC THRESHOLD —VS— SUPPLY VOLTAGES

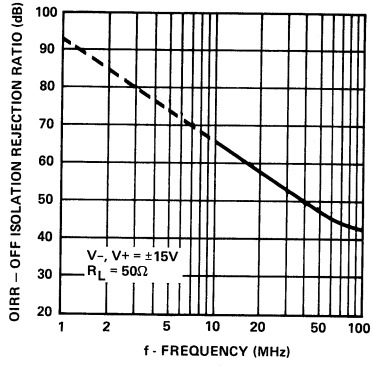


SUPPLY CURRENTS —VS— AMBIENT TEMPERATURE

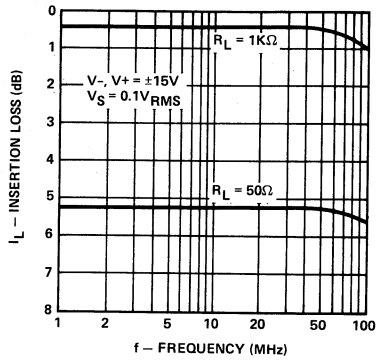


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

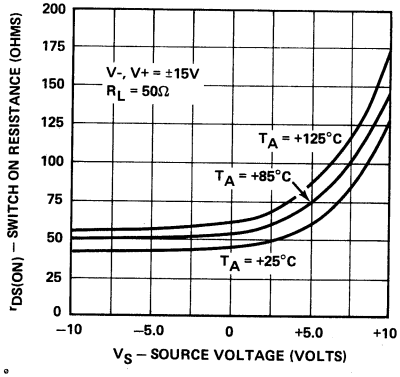
SWITCH-OFF ISOLATION REJECTION RATIO —VS— FREQUENCY



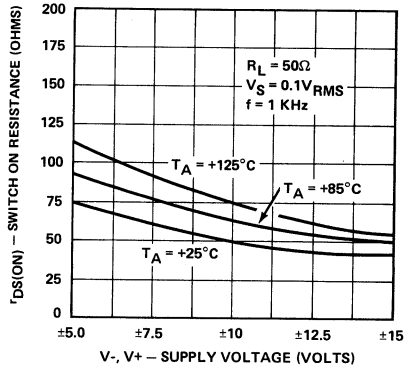
INSERTION LOSS —VS— FREQUENCY



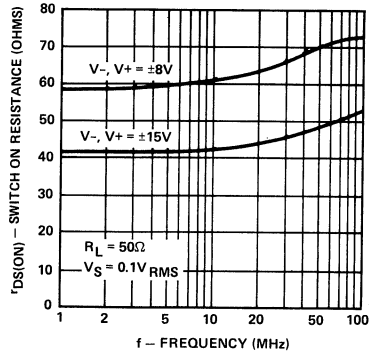
SWITCH ON RESISTANCE —VS— ANALOG VOLTAGE



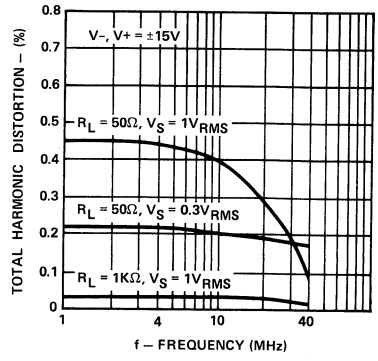
SWITCH-ON RESISTANCE —VS— SUPPLY VOLTAGES



SWITCH-ON RESISTANCE —VS— FREQUENCY



TOTAL HARMONIC DISTORTION —VS— FREQUENCY



TOPAZ SEMICONDUCTOR

CDG211

QUAD MONOLITHIC SPST CMOS/D-MOS ANALOG SWITCH

ORDERING INFORMATION

Quad SPST Switch, Logic '0' ON, Break-before-make	16-Pin Plastic DIP
Commercial Temp. Range	CDG211CJ

FEATURES

- High OFF Isolation, 66 dB @ 10MHz
- Wide Bandwidth Switches, 0.9 x DC @ 100MHz
- Low Channel-to-Channel Cross Talk, -80 dB @ 10MHz
- TTL Compatible
- Low 'OFF' Leakage
- Industry Standard Pin-Out

APPLICATIONS

- Glitch-Free Analog Switches
- RF & Video Switches
- Track and Hold Switches
- Sample and Hold Switches

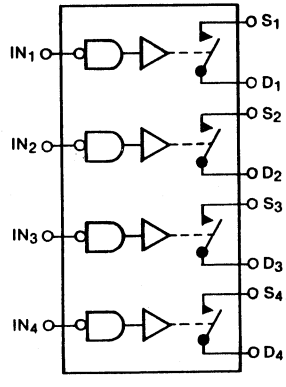
DESCRIPTION

The Topaz Semiconductor CDG211 low cost Analog Switch features TTL compatible input logic and wide-band Lateral D-MOS switches on a single chip. The on-chip reference used for TTL compatibility gives the added advantage of constant logic switching over a wide range of supply voltages and temperature without a separate power supply. Industry standard pin-out makes the CDG211 particularly suitable for replacement of existing analog switches and at the same time upgrading high frequency performance.

NOTE

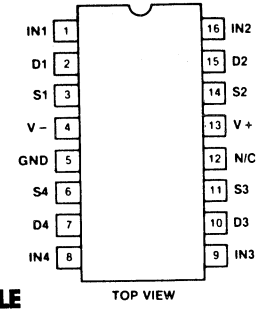
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (V_{DD} or GND).

FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches per Package
Switches shown in Logic "1" Input Position

PIN CONFIGURATION



TOP VIEW

LOGIC TABLE

Logic	Switch
0	ON
1	OFF

Logic '0' ≦ 0.8V
Logic '1' ≧ 2.4V

ABSOLUTE MAXIMUM RATINGS

V- Negative Supply Voltage ..... -20V
V+ Positive Supply Voltage ..... +20V
V_{IN} Control Input Voltage Range ..... V+ +0.3V, V- -0.3V
I_L Continuous Current, any Pin Except S or D ..... 30 mA
I_S Continuous Current, S or D ..... 30 mA
I_S Peak Pulsed Current, S or D, 80μsec, 1%, Duty Cycle ..... 90 mA
T_S Storage Temperature Range ..... -55 to +125°C
P_D Power Dissipation (derate at 5.5mW/°C, above +70°C) ..... 500 mW

RECOMMENDED OPERATING CONDITIONS

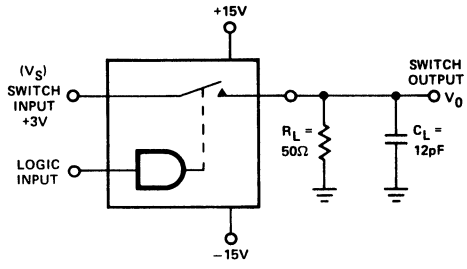
V- Negative Supply Voltage ..... -8.0 to -15V
V+ Positive Supply Voltage ..... +8.0 to +15V
V_{IN} Control Input Voltage Range ..... 0 to +5V
V_S Analog Switch Voltage Range ..... -10 to +10V
T_{OP} Operating Temperature (C Suffix) .... 0 to +70°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V- = -15V, V+ = +15V unless otherwise noted)

#	SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	STATIC	V_{ANALOG}	Analog Signal Range	-10		+10	V		
2		$r_{DS(on)}$	Switch ON Resistance		40	80	Ω	V_S = -10V	V_{IN} = 0
3					45	80		V_S = +2.0V	
4					100	160		V_S = +10V	
5		V_{IH}	High Level Input Voltage	2.4			V		
6		V_{IL}	Low Level Input Voltage			0.8			
7		I_{IN}	Logic Input Leakage Current		0.01	0.1	μA	V_{IN} = +2.4V	
8					0.02	0.1		V_{IN} = +15V	
9		$I_{D(OFF)}$	Switch OFF Leakage Current		0.2	5.0	nA	V_D = +10V, V_S = -10V	V_{IN} = +2.4V
10		$I_{S(OFF)}$			0.4	5.0		V_S = +10V, V_D = -10V	
11		I-	Negative Supply Quiescent Current		-0.3	-1.0	mA	V_{IN} = 0 or +2.4V	
12		I+	Positive Supply Quiescent Current		0.6	2.0			
13	DYNAMIC	t_{ON}	Switch Turn-On Time		400	600	nSec	See Switching Times Test Circuit	
14		t_{OFF}	Switch Turn-OFF Time		70	300			
15		O_{IRR}	OFF Isolation, Rejection Ratio	60	66		dB	f = 10 MHz R_L = 50Ω	
16		C_{CRR}	Cross-Coupling Rejection Ratio		80				
17		C_d	Drain-Node Capacitance		0.3		pF	V_D = V_S = 0 f = 1MHz	V_{IN} = +2.4V
18		C_s	Source-Node Capacitance		3.0				

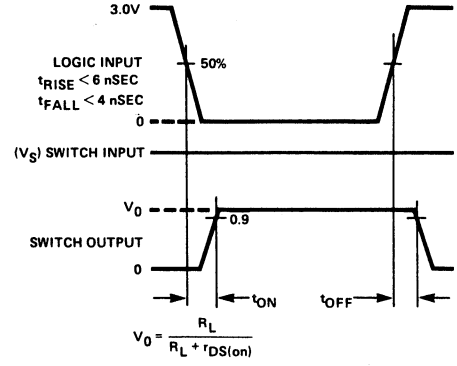
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

SWITCHING TIMES TEST CIRCUIT

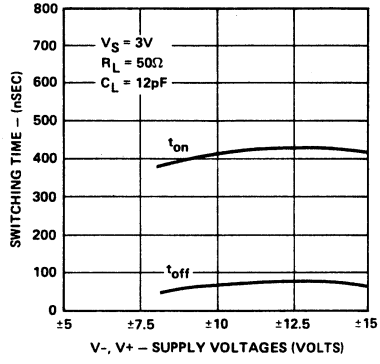


SWITCH ILLUSTRATED IN LOGIC "1", SWITCH OFF, POSITION

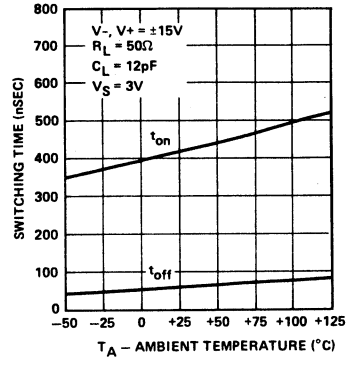
TEST WAVEFORMS



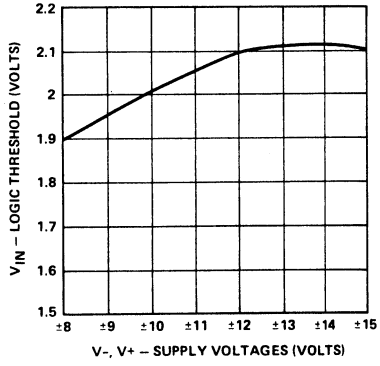
SWITCHING TIMES —VS— SUPPLY VOLTAGES



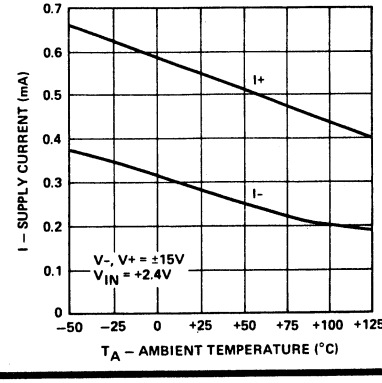
SWITCHING TIMES —VS— AMBIENT TEMPERATURE



LOGIC THRESHOLD —VS— SUPPLY VOLTAGES

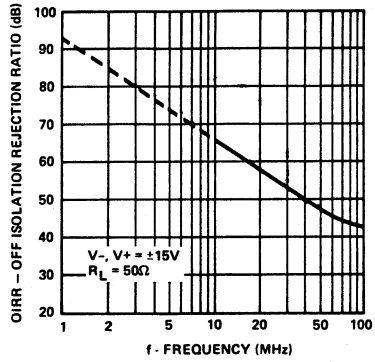


SUPPLY CURRENTS —VS— AMBIENT TEMPERATURE

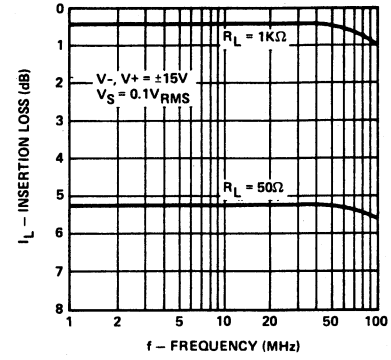


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

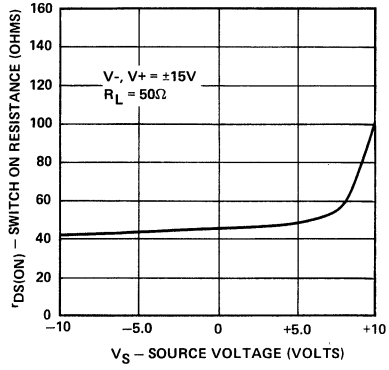
SWITCH-OFF ISOLATION REJECTION RATIO —VS— FREQUENCY



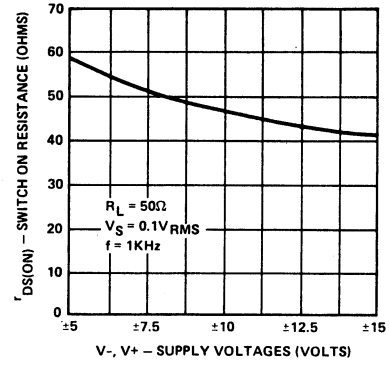
INSERTION LOSS —VS— FREQUENCY



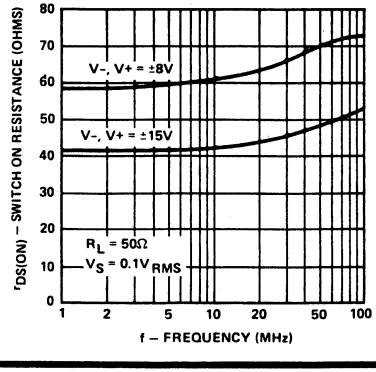
SWITCH ON RESISTANCE —VS— ANALOG VOLTAGE



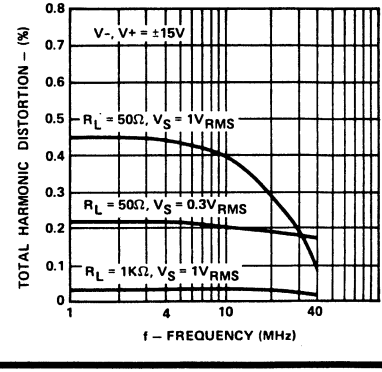
SWITCH-ON RESISTANCE —VS— SUPPLY VOLTAGES



SWITCH-ON RESISTANCE —VS— FREQUENCY



TOTAL HARMONIC DISTORTION —VS— FREQUENCY



TOPAZ SEMICONDUCTOR

CDG308, CDG309 CDG4308, CDG4309

QUAD MONOLITHIC SPST CMOS/D-MOS ANALOG SWITCHES

ORDERING INFORMATION

Quad SPST Break-before-make	16-Pin Plastic DIP		16-Pin Ceramic DIP		20-Pin Plastic DIP	
Commercial Temp. Range	CDG308CJ	CDG309CJ	—	—	—	—
Industrial Temp. Range	CDG308BJ	CDG309BJ	CDG308BK	CDG309BK	CDG4308BJ	CDG4309BJ
Military Temp. Range	—	—	CDG308AK	CDG309AK	—	—
Logic '0' ≤ 1.0V Logic '1' ≥ 4.5V	Logic '1' ON	Logic '1' OFF	Logic '1' ON	Logic '1' OFF	Logic '1' ON	Logic '1' OFF

FEATURES

- High Off Isolation, 68dB @ 10MHz
- Low Insertion Loss, 0.9 x DC @ 100MHz
- Low Channel-to-Channel Cross Talk, -80dB @ 10MHz
- CMOS Compatible Inputs
- Low 'OFF' Leakage
- Industry Standard Pin-Out, CDG308/309

APPLICATIONS

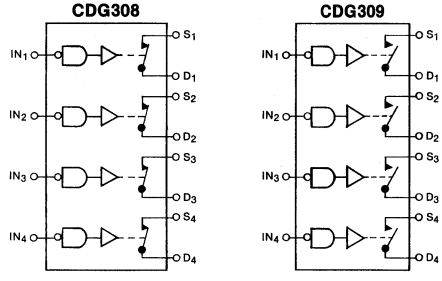
- Glitch-Free Analog Switches
- RF & Video Switches
- Track and Hold Switches
- Sample and Hold Switches

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Switches feature high-speed, low-power CMOS input logic and level translation circuitry and high-speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip. The CDG4308 and CDG4309 use the same die as CDG308 and CDG309; the extra isolating pin between switch input and output increases isolation by 6 dB.

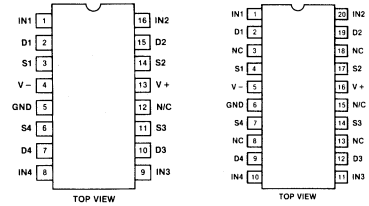
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{DD} or GND).

FUNCTIONAL BLOCK DIAGRAMS



Four SPST Switches per Package
Switches Shown in Logic "1" Input Position

PIN CONFIGURATIONS



CDG308
CDG309

CDG4308
CDG4309

LOGIC TABLE

Logic	CDG308 CDG4308	CDG309 CDG4309
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS

$V-$ Negative Supply Voltage ..... -20V
$V+$ Positive Supply Voltage ..... +20V
V_{IN} Control Input Voltage Range ..... V+ +0.3V, V- -0.3V
I_L Continuous Current, any Pin Except S or D ..... 20 mA
I_S Continuous Current, S or D ..... 30 mA
I_S Peak Pulsed Current, S or D, 80μsec, 1%, Duty Cycle ..... 180 mA
T_J Junction Temperature Range ..... -55 to +125°C
T_S Storage Temperature Range ..... -55 to +125°C
P_D Power Dissipation (derate at 12mW/°C, above +85°C) ..... 500 mW

RECOMMENDED OPERATING CONDITIONS

$V-$ Negative Supply Voltage ..... -8.0 to -15V
$V+$ Positive Supply Voltage ..... +8.0 to +15V
V_{IN} Control Input Voltage Range ..... 0 to +5V
V_S Analog Switch Voltage Range ..... -10 to +10V
T_{OP} Operating Temperature
(A Suffix) ..... -55 to +125°C
(B Suffix) ..... -25 to +85°C
(C Suffix) ..... 0 to +70°C

ELECTRICAL CHARACTERISTICS ($V-$ = -15V, $V+$ = +15V per channel unless otherwise noted, T_A = +25°C)

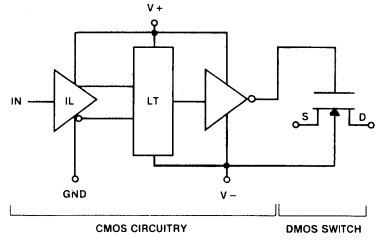
#	SYMBOL		PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	V_{ANALOG}	Analog Signal Range		-10		+10	V	
2		$r_{DS(on)}$	Switch ON Resistance			40	80	ohms	V_S = -10V
3						45	80		V_S = +2.0V
4						100	160		V_S = +10V
5		V_{IH}	High Level Input Voltage		4.5	3.4		V	
6		V_{IL}	Low Level Input Voltage				1.0		
7		I_{IN}	Logic Input Leakage Current			0.01	0.1	μA	V_{IN} = +5.0V
8						0.02	0.1		V_{IN} = +15V
9		$I_{D(off)}$	Switch OFF Leakage Current			0.2	5.0	nA	V_D = +10V, V_S = -10V; CDG309/4309
10		$I_{S(off)}$				0.4	5.0		V_S = +10V, V_D = -10V; V_{IN} = 5.0V
11		I-	Neg. Supply Quiescent Current			-0.1	-0.5	μA	CDG308/4308
12		I+	Pos. Supply Quiescent Current			0.1	0.5		V_{IN} = 1.0V
13	DYNAMIC	t_{on}	Switch Turn-On Time			140	250	nSec	V_{IN} = 1.0V CDG308, CDG4308
14		t_{off}	Switch Turn-Off Time			80	220		V_{IN} = 5.0V CDG309, CDG4309
15		O_{IRR}	Off Isolation	CDG308/309	60	62		dB	f = 10MHz
16			Rejection Ratio	CDG4308/4309	66	68			R_L = 50Ω
17		C_{CRR}	Cross-Coupling Rejection Ratio			80		dB	f = 10MHz, R_L = 50Ω
18		c_d	Drain-Node Capacitance			0.3		pF	V_{IN} = 1.0V CDG308, CDG4308
19		c_s	Source-Node Capacitance			3.0			V_{IN} = 5.0V, CDG309, CDG4309; V_D = V_S = 0, f = 1MHz

ELECTRICAL CHARACTERISTICS ($V-$ = -15V, $V+$ = +15V, per channel)

LIMITS AT TEMPERATURE EXTREMES

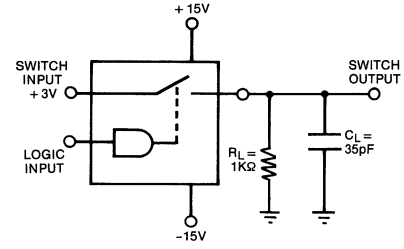
#	SYMBOL		PARAMETER	MAXIMUM @ T_A = -55°C	-25°C	+70°C	+85°C	+125°C	UNITS	TEST CONDITIONS
1	STATIC	V_{ANALOG}	Analog Signal Range	±10	±10	±10	±10	±10	V	
2		$r_{DS(on)}$	Switch On Resistance	80	80	120	120	150	ohms	V_S = -10V
3				80	80	120	120	150		V_S = +2.0V
4				160	160	240	240	300		V_S = 10V
5		I_{IN}	Logic Input Leakage Current	0.1	0.1	1.0	1.0	10	μA	V_{IN} = +5.0V
6				0.1	0.1	2.0	2.0	20		V_{IN} = +15V
7		$I_{D(OFF)}$	Switch OFF Leakage Current	5.0	5.0	100	100	1000	nA	V_D= +10V, V_S = -10V
8		$I_{S(OFF)}$		5.0	5.0	100	100	1000		V_S = +10V, V_D = -10V
9		I-	Supply Quiescent Currents	-0.5	-0.5	-20	-20	-100	μA	
10		I+		0.5	0.5	20	20	100		

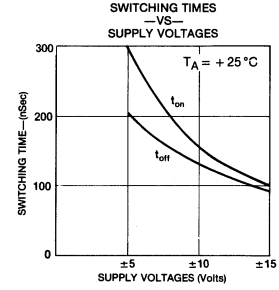
FUNCTIONAL DIAGRAM (1 of 4 channels)



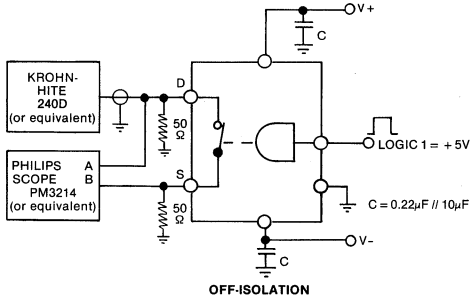
Switch Contacts:
Switches are bi-directional (Analog Input can be to Source or Drain). However, for optimum performance in Video Applications, connect Input to Source and Output to Drain.

SWITCHING TIMES TEST CIRCUIT

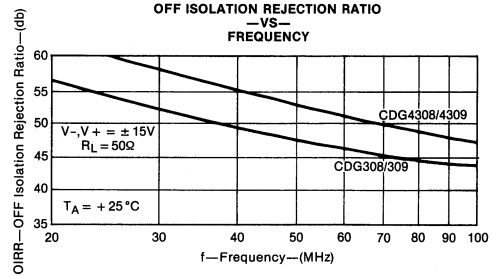




OFF ISOLATION TEST CIRCUIT

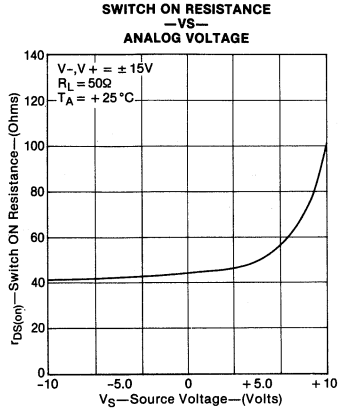


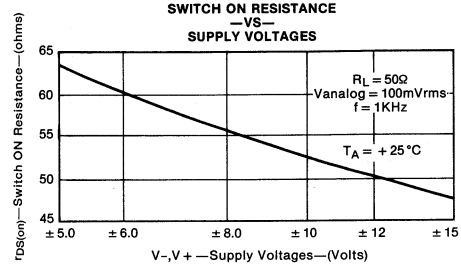
OFF-ISOLATION



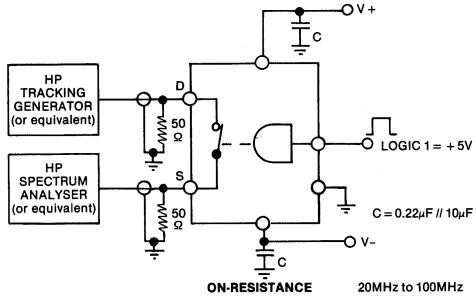
CHANNEL-TO-CHANNEL CROSSTALK TEST CIRCUIT

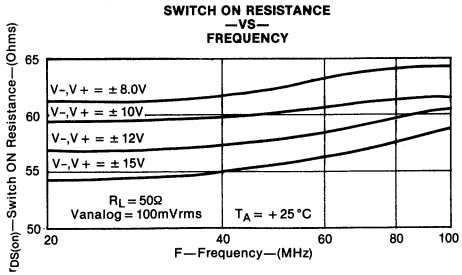
SWITCH ON RESISTANCE

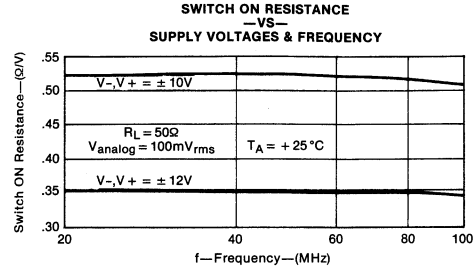




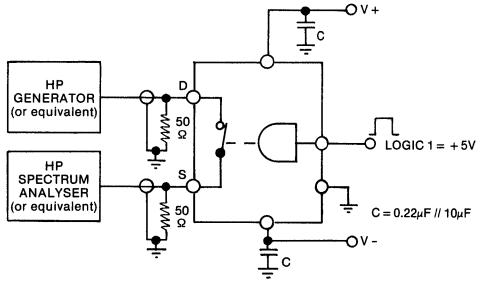
SWITCH ON RESISTANCE —VS— FREQUENCY TEST CIRCUIT





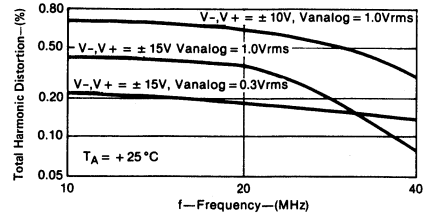


DISTORTION —VS— FREQUENCY

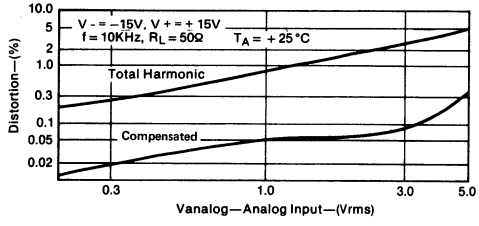


HARMONIC DISTORTION 10MHz-40MHz

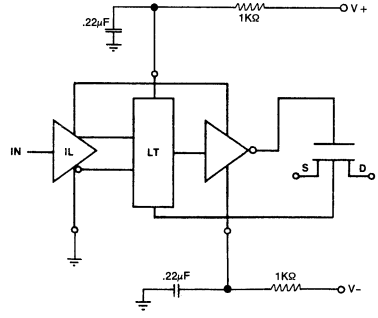
TOTAL HARMONIC DISTORTION
—VS—
FREQUENCY



DISTORTION
—VS—
ANALOG INPUT VOLTAGE

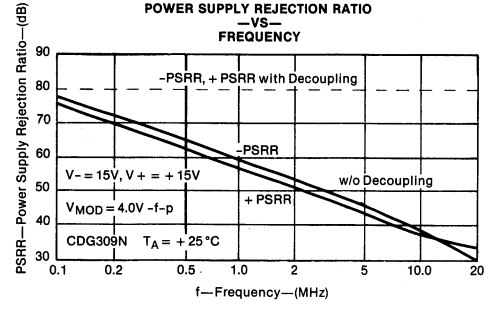


POWER SUPPLY REJECTION RATIO
POWER SUPPLY DECOUPLING CIRCUIT



By inserting 1K ohm resistors in series with V+ and V- power supply lines and decoupling both pins at the device socket, it is possible to improve power supply rejection ratios of a video switch by 50dB at frequencies of 20MHz and higher.

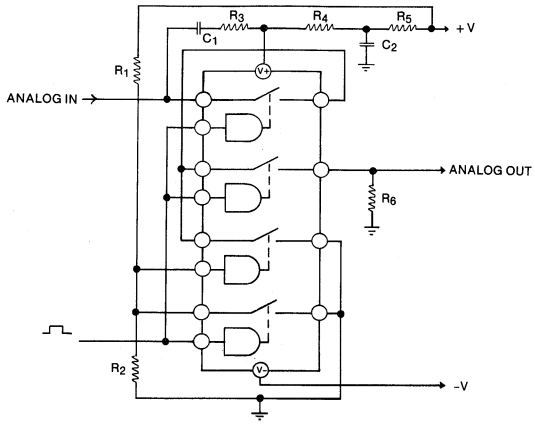
POWER SUPPLY REJECTION RATIO
—VS—
FREQUENCY



APPLICATIONS

LOW DISTORTION, RAIL-TO-RAIL ANALOG SWITCH

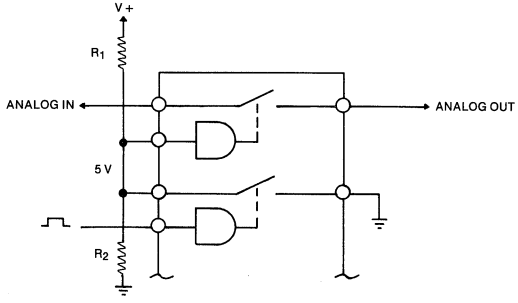
Features very low distortion for low frequency and large signal applications.



VERY LOW DISTORTION CIRCUIT FOR LOW FREQUENCY AND LARGE SIGNAL APPLICATIONS

This circuit provides very low distortion (< 0.1%) and high off isolation (> 90dB) at signal levels equal to the supply voltage. The signal passes through a T switch configuration and at the same time is modulating the power supply. This modulation maintains a constant on resistance $r_{DS(on)}$ which in turn reduces the distortion. R5 is for bypassing the power supply and has a typical value of 1K ohm, R4 should be a value that can be accommodated by the signal source as load, R3 is only necessary at loads lower than 100 ohms and should be selected during the initial design of the circuit, C1 has to be large enough for the lowest signal to pass and C2 will have to bypass all signals. R1 and R2 set up the one logic level for the control input and should be set to 5 volts.

LOGIC INVERTER



This circuit provides logic inversion with two resistors and one switch. It does not require additional logic parts. The resistors divide the supply voltage down to a 5 volt level when high and are switched to a low level via the switch. This configuration allows a single pole, single throw switch to be changed into a single pole, double throw switch.

TOPAZ SEMICONDUCTOR

CDG2214

HIGH SPEED ANALOG SWITCH

FEATURES

- Ultra High OFF Isolation, > 40 dB @ 100MHz and > 25 dB @ 200 MHz
- High Speed Switching, t_{on} 40 nS and t_{off} 20 nS
- CMOS Compatible Inputs
- Low ON Resistance, <50Ω
- Wide Bandwidth, -3 dB @ 250MHz

APPLICATIONS

- RF & Video Switches
- High Frequency Data Acquisition
- High Frequency Multiplexers

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Switches feature high-speed, low-power CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip.

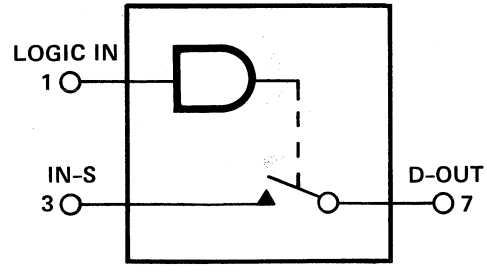
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{cc} or GND).

ORDERING INFORMATION

One SPST Switch Break-before-make	8-Pin Plastic Dip
Industrial Temperature Range	CDG2214BJ

Available in Chip form.
Contact factory for Ordering Information.

FUNCTIONAL DIAGRAM

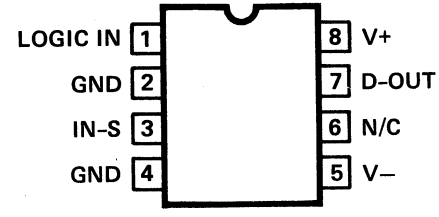


One SPST Switch per Package.

Switch shown in Logic "1" Input Position.

Logic '0' ≤ 1.0V
Logic '1' ≥ 4.5V

PIN CONFIGURATION



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

V_- Negative Supply Voltage ..... -20V
V_+ Positive Supply Voltage ..... +20V
V_{IN} Control Input Voltage Range ..... V+ +0.3V, V- -0.3V
I_L Continuous Current, any Pin Except S or D ..... 20 mA
I_S Continuous Current, S or D ..... 40 mA
I_S Peak Pulsed Current, S or D, 80μsec, 1%, Duty Cycle ..... 100 mA
T_J Junction Temperature Range ..... -55 to +125°C
T_S Storage Temperature Range ..... -55 to +125°C
P_D Power Dissipation (derate at 12mW/°C, above +85°C) ..... 500 mW

RECOMMENDED OPERATING CONDITIONS

V_- Negative Supply Voltage ..... -5 to -15V
V_+ Positive Supply Voltage ..... +5 to +15V
V_{IN} Control Input Voltage Range ..... 0 to +5V
T_{OP} Operating Temperature (B Suffix) ..... -25 to +85°C

ELECTRICAL CHARACTERISTICS (V_- = -15V, V_+ = +15V unless otherwise noted, T_A = +25°C)

#	SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
1	V_{ANALOG}	STATIC	Analog Signal Range	-10		+10	V		
2	$r_{DS(on)}$	STATIC	Switch ON Resistance		45	80	Ω	V_S = -10V	
3		STATIC			50	80		V_S = +2.0V	
4		STATIC			130	160		V_S = +10V	
5	V_{IH}	STATIC	High Level Input Voltage	4.5	3.4		V		
6	V_{IL}	STATIC	Low Level Input Voltage			1.0			
7	I_{IN}	STATIC	Logic Input Leakage Current		0.01	0.1	μA	V_{IN} = +5.0V	
8		STATIC			0.02	0.1		V_{IN} = +15V	
9	$I_{D(OFF)}$	STATIC	Switch OFF Leakage Current		0.2	5.0	nA	V_D = +10V, V_S = -10, V_{IN} = 5V	
10	$I_{S(OFF)}$	STATIC			0.2	5.0		V_S = +10V, V_D = -10, V_{IN} = 5V	
11	I-	STATIC	Negative Supply Quiescent Current			-8.0	mA	V_{IN} = 0 or V+	
12	I+	STATIC	Positive Supply Quiescent Current			8.0			
13	t_{ON}	DYNAMIC	Switch Turn-On Time		40	60	nsec	V_{IN} = 5.0V, R_L = 50Ω	
14	t_{OFF}	DYNAMIC	Switch Turn-OFF Time		20	40		C_L = 12 pF	
15	O_{IRR}	DYNAMIC	OFF Isolation Rejection Ratio	37	40		dB	R_L = 50Ω	f = 100 MHz
16		DYNAMIC		22	25				f = 200 MHz
17	I_L	DYNAMIC	Insertion Loss		7.8	13	dB	R_L = 50Ω, f = 200 MHz	
18	C_d	DYNAMIC	Drain-Node Capacitance		0.3		pF	V_D = 0	f = 1MHz, V_{IN} = 0
19	C_s	DYNAMIC	Source-Node Capacitance		3.0			V_S = 0	

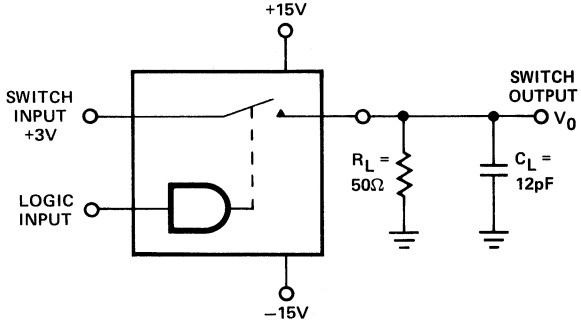
ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel unless otherwise noted)

LIMITS AT TEMPERATURE EXTREMES

#	SYMBOL		PARAMETER	MAXIMUM		UNITS	TEST CONDITIONS
				T_A = -25°C	T_A = +85°C		
1	V_{ANALOG}	STATIC	Analog Signal Range	±10	±10	V	
2	$r_{DS(on)}$	STATIC	Switch On Resistance	80	120	Ω	V_S = -10V
3				80	120		V_S = +2.0V
4				160	240		V_S = +10V
5	I_{IN}	STATIC	Logic Input Leakage Current	0.1	1.0	μA	V_{IN} = +5.0V
6				0.1	2.0		V_{IN} = +15V
7	$I_{D(OFF)}$	STATIC	Switch OFF Leakage Current	5.0	200	nA	V_D = +10V, V_S = -10V, V_{IN} = 5V
8	$I_{S(OFF)}$	STATIC		5.0	200		V_S = +10V, V_D = -10V, V_{IN} = 5V
9	I-	STATIC	Negative Supply Quiescent Current	-8.0	-10	mA	V_{IN} = 0 or V+
10	I+	STATIC	Positive Supply Quiescent Current	8.0	10		

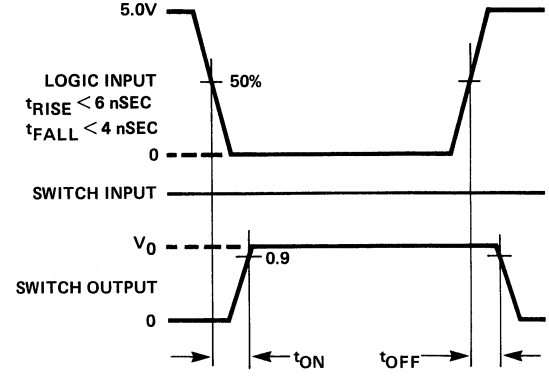
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

SWITCHING TIMES TEST CIRCUIT

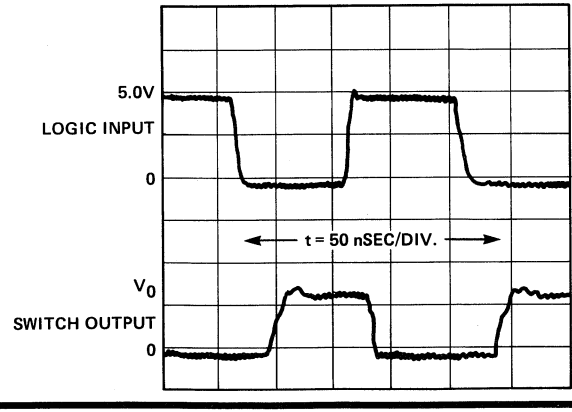


SWITCH ILLUSTRATED IN LOGIC "1", SWITCH OFF, POSITION

TEST WAVEFORMS

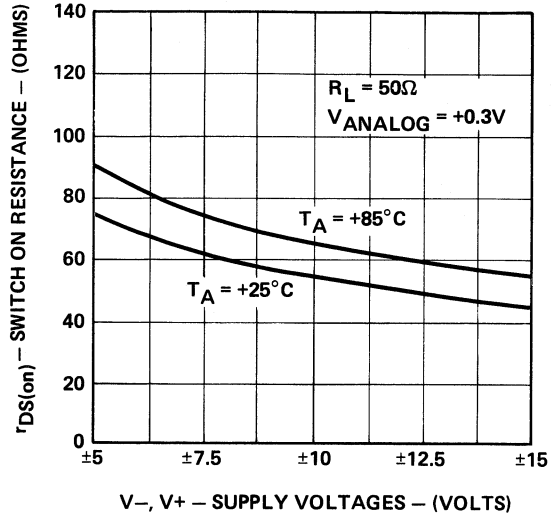


TEST RESULTS

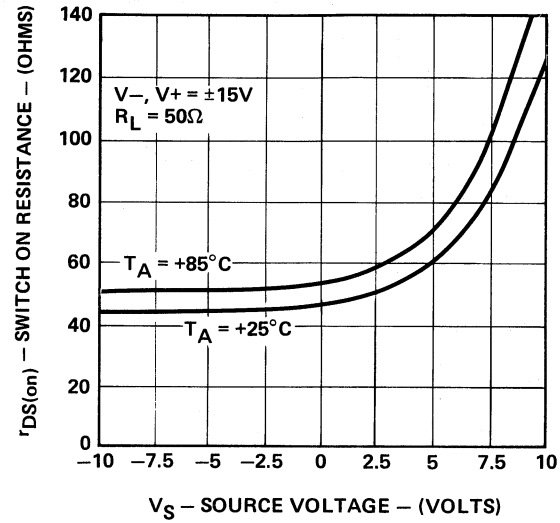


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

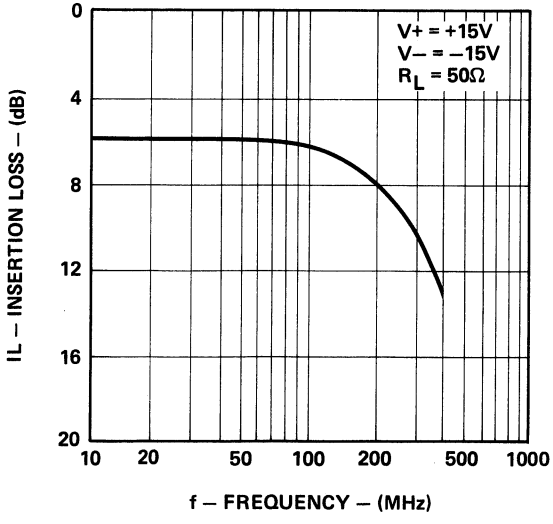
SWITCHING ON RESISTANCE —VS— SUPPLY VOLTAGES



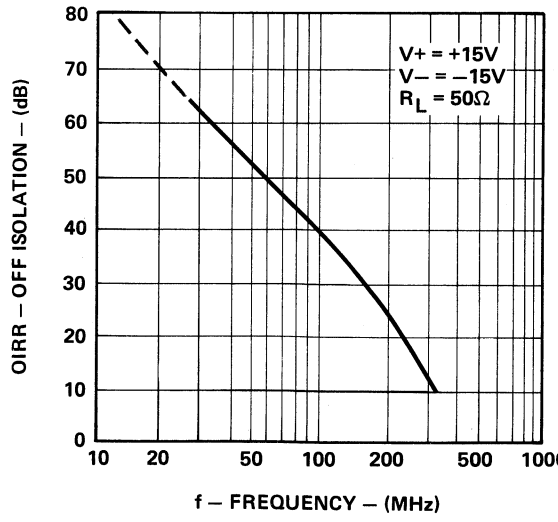
SWITCHING ON RESISTANCE —VS— ANALOG VOLTAGE



INSERTION LOSS —VS— FREQUENCY



OFF ISOLATION —VS— FREQUENCY



TOPAZ SEMICONDUCTOR

CDG4469

8-BIT HIGH FREQUENCY DIGITAL CONTROLLED ATTENUATOR

FEATURES

- Input Voltage up to 6.0V_{RMS}
- Attenuation Range of 0 to 127.5dB
- Precise Attenuation Selectable in 0.5dB steps
- Wide Frequency Range, up to 15MHz
- Constant Input Impedance of 650 ohms
- Wide Power Supply Range, ±6.0 to ±15V
- Lower Power Consumption, 0.5μW typ. with ±15V Power Supplies

APPLICATIONS

- Video Attenuation
- Digital Amplifier Gain Control
- Variable Burst Generation
- Log D/A Conversion
- Frequency Synthesizers

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS high frequency attenuators feature high-speed, low-power CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on single silicon chips and mounted on hybrid circuit substrates with precision trimmed resistors.

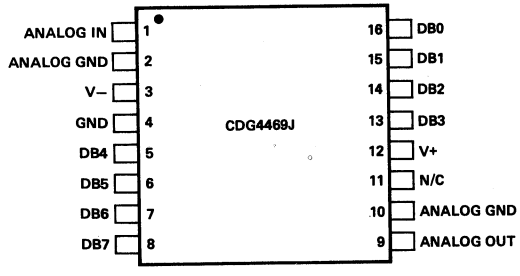
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level.

ORDERING INFORMATION

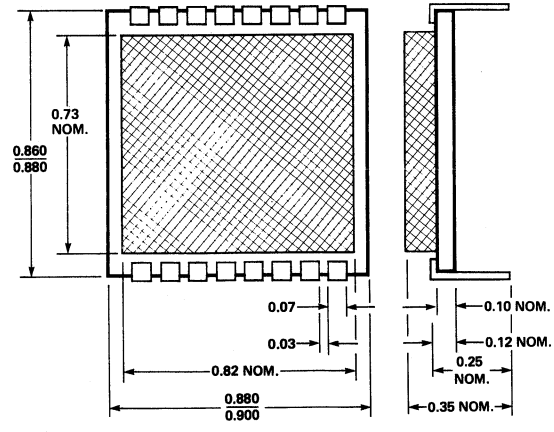
16-Pin Ceramic Package	CDG4469J

PIN CONFIGURATION

TOP VIEW

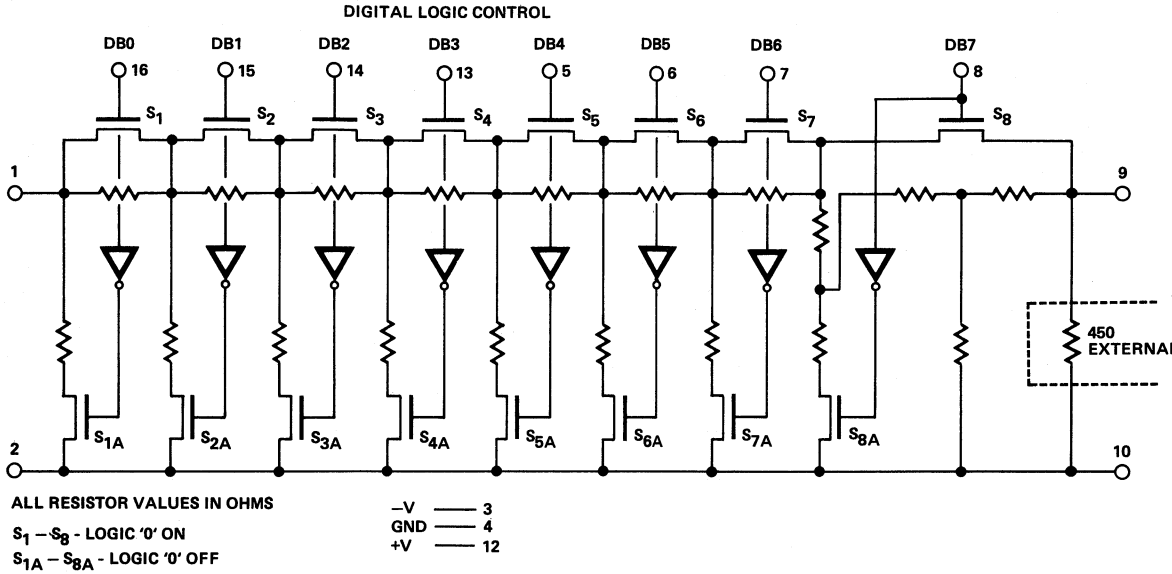


PACKAGE DIMENSIONS



ALL DIMENSIONS IN INCHES

SCHEMATIC DIAGRAM



ATTENUATOR SETTING TABLE

Note: Examples only. Added attenuation value can be set between 0 and 127.5 dB in 0.5 dB steps.

ADDED ATTENUATION (dB)	DATA BIT #—LOGIC SETTING							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
0.5	1	0	0	0	0	0	0	0
1.0	0	1	0	0	0	0	0	0
2.0	0	0	1	0	0	0	0	0
4.0	0	0	0	1	0	0	0	0
8.0	0	0	0	0	1	0	0	0
16	0	0	0	0	0	1	0	0
32	0	0	0	0	0	0	1	0
64	0	0	0	0	0	0	0	1

EXAMPLES OF OTHER ATTENUATION SETTINGS

1.5	1	1	0	0	0	0	0	0
3.5	1	1	1	0	0	0	0	0
15.5	1	1	1	1	1	0	0	0
31.5	1	1	1	1	1	1	0	0
63.5	1	1	1	1	1	1	1	0
127.5	1	1	1	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS

V-, V+	Supply Voltages	±20V
V_{IN}	Control Input Voltage Range	V- to V+
V_A	Analog Input Voltage	±8.0V
I	Continuous Current, any Pin	20mA
T_J	Junction Temperature Range	-55 to +125°C
T_S	Storage Temperature Range	-55 to +125°C
P_D	Power Dissipation	600mW

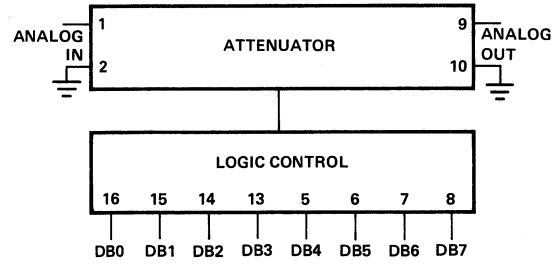
RECOMMENDED OPERATING CONDITIONS

V-, V+	Supply Voltage Ranges	±6.0V to ±15V
V_{IN}	Control Input Voltage Range	0 to +5V
V_A	Analog Input Voltage	±8.0V
T_{OP}	Operating Junction Temperature Range	-40 to +85°C

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, T_A = +25°C)

#	SYMBOL		PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	STATIC	V_{IH}	High Level Input Voltage	5.0	3.4		V	
2		V_{IL}	Lower Level Input Voltage			1.0		
3		I_{IN}	Logic Input Leakage Current		0.01	0.1	μA	V_{IN} = +5.0V
4					0.02	0.1		V_{IN} = +15V
5		I-	Negative Supply Quiescent Current		-0.5	-10	μA	V_{IN} = 0 or V+
6		I+	Positive Supply Quiescent Current		0.5	10		
7	DYNAMIC		Insertion Loss		3.9	4.5	dB	R_{IN} = 650 Ω, R_L = 450 Ω Attenuation Setting=0dB
8		t_{on}	Turn-ON Time		140	250	nS	V_{IN} = 5.0V
9		t_{off}	Turn-OFF Time		100	220		

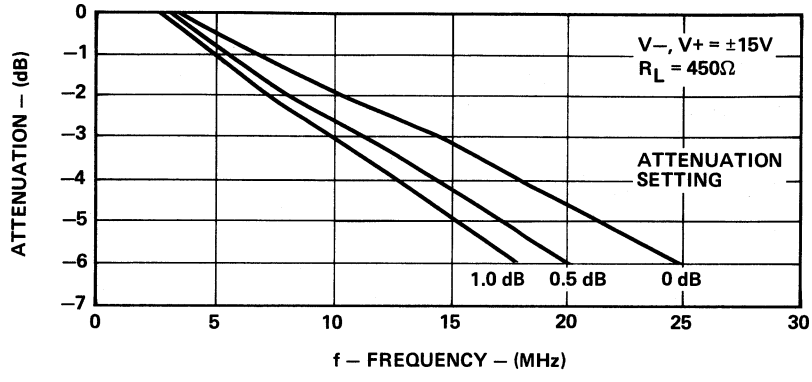
BLOCK DIAGRAM



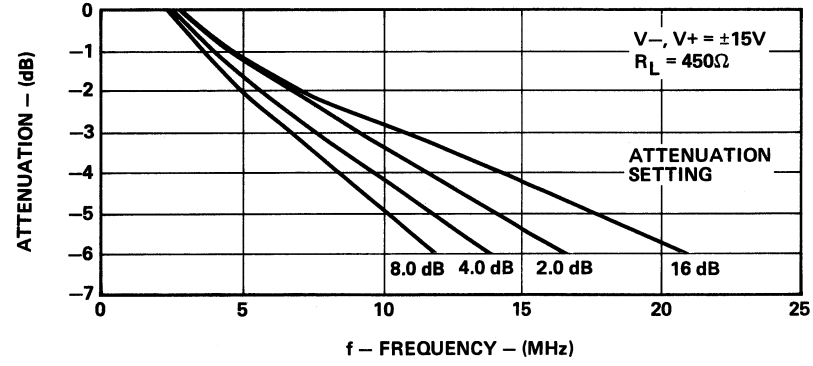
All Data Bit Pins must be connect to logic '0' or Logic '1' input according to Attenuation Setting.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C)

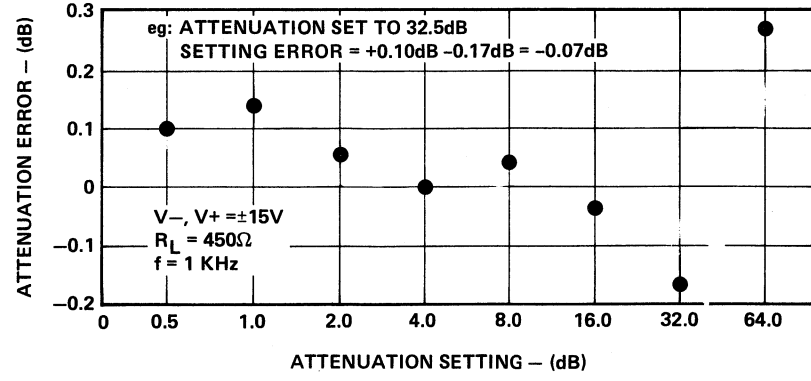
FREQUENCY RESPONSE vs ATTENUATION



FREQUENCY RESPONSE vs ATTENUATION

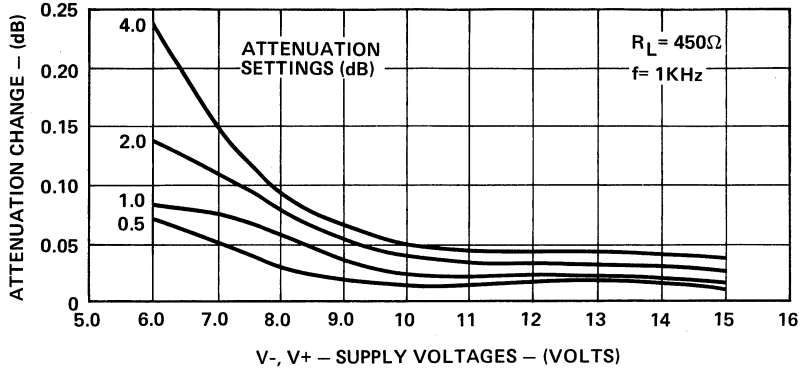


ATTENUATION ERROR vs ATTENUATION SETTING

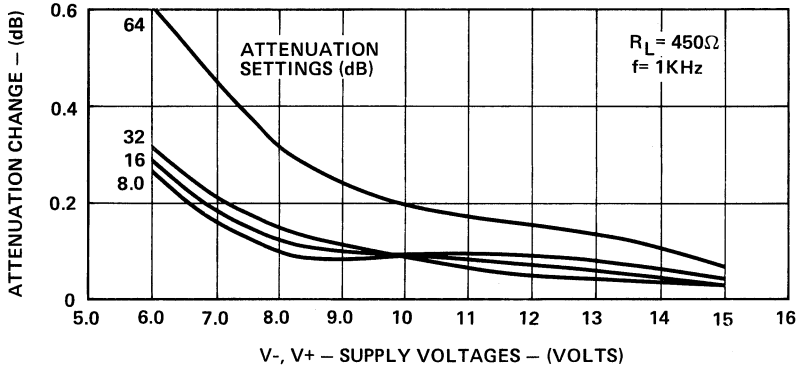


TYPICAL PERFORMANCE CHARACTERISTICS (Cont) (T_A = +25°C)

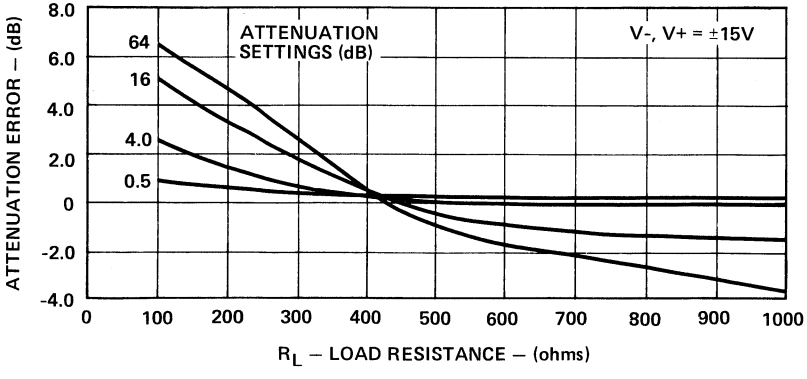
ATTENUATION CHANGE vs SUPPLY VOLTAGES



ATTENUATION CHANGE vs SUPPLY VOLTAGES

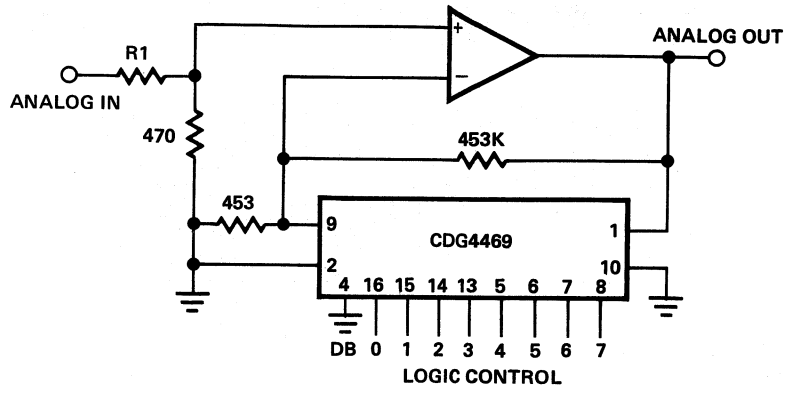


ATTENUATOR ERROR vs LOAD RESISTANCE



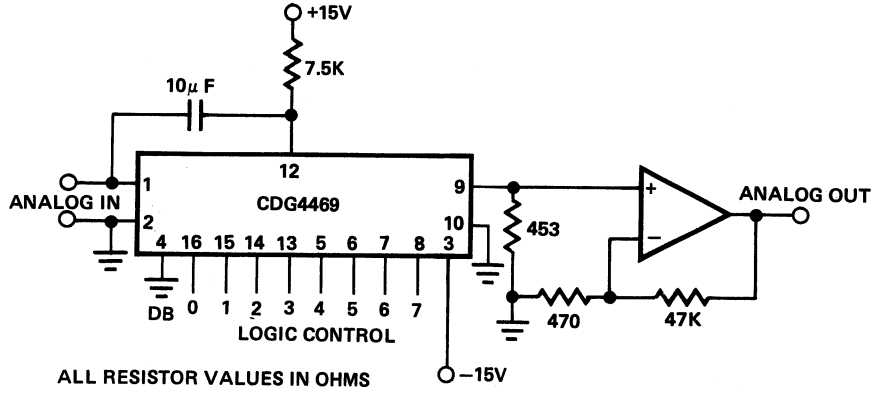
APPLICATIONS

GAIN CONTROL Ø to +60dB



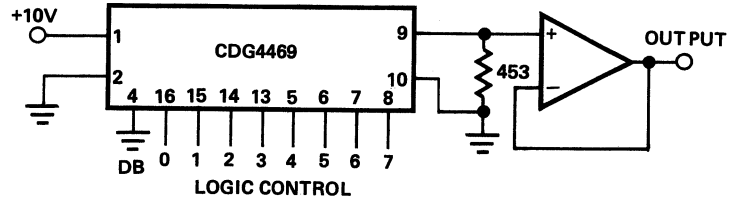
ALL RESISTOR VALUES IN OHMS
R_1 – 0 dB ADJUST

ATTENUATOR/AMPLIFIER



ALL RESISTOR VALUES IN OHMS
RANGE – +40 TO -87.5 dB
FREQUENCY – UP TO 500KHz

LOG D-A CONVERTER



TOPAZ SEMICONDUCTOR

CDG4500

4-CHANNEL CMOS/D-MOS HIGH-FREQUENCY MULTIPLEXER

ORDERING INFORMATION

4-Channel Multiplexer with Enable	14-Pin Plastic DIP	14-Pin Ceramic DIP
Commercial Temp. Range	CDG4500 CJ	—
Industrial Temp. Range	CDG4500 BJ	CDG4500 BK
Military Temp. Range	—	CDG4500 PIK

FEATURES

- High OFF Isolation, >62dB @ 10 MHz
- Low Channel-to-Channel Crosstalk, >80dB @ 10 MHz
- 5 Volt CMOS Compatible Inputs
- Low ON Resistance, 40 Ω typ.
- Wide Bandwidth, -3.0dB @ 100 MHz
- Wide Analog Signal Range +10V to -10V
- High Speed Logic Control

APPLICATIONS

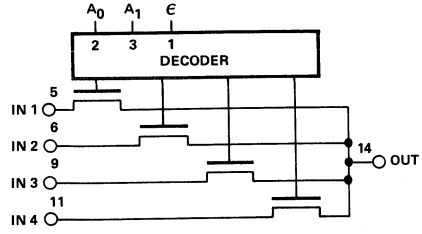
- RF & Video Switches
- High Speed Precision Data Acquisition

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Multiplexer feature high-speed, low-power 5 volt CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip. This part is designed for applications where high "off" isolation at high frequencies is needed. The 14 pin configuration gives a compact board layout without impacting "off" isolation and by use of the enable allows higher levels of multiplexing.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{CC} or GND).

FUNCTION DIAGRAM

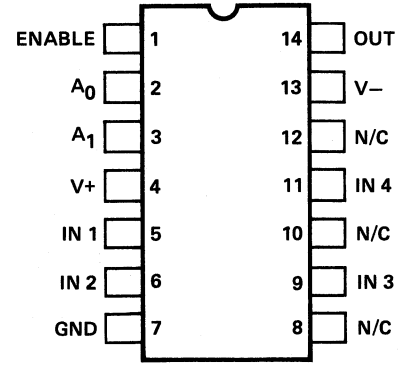


FUNCTION TABLE

ENABLE	A_0	A_1	CHANNEL
H	x	x	OFF
L	L	L	S_1
L	H	L	S_2
L	L	H	S_3
L	H	H	S_4

x = UNDEFINED

PIN CONFIGURATION



TOP VIEW

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799, 408/942-9100 TWX: 910-338-0025

ABSOLUTE MAXIMUM RATINGS

V–	Negative Supply Voltage	-20V
V+	Positive Supply Voltage	+20V
V_{IN}	Control Input Voltage Range	V+ +0.3V, V– –0.3V
I_L	Continuous Current, any Pin except S or D	20mA
I_S	Continuous Current, S or D	30mA
I_S	Peak Pulsed Current, S or D, 80μsec, 1% Duty Cycle	100mA
T_J	Junction Temperature Range	–55 to +125°C
T_S	Storage Temperature Range	–55 to +125°C
P_D	Power Dissipation (derate at 12mW/°C, above +85°C)	500mW

RECOMMENDED OPERATING CONDITIONS

V–	Negative Supply Voltage	–8.0 to –15V
V+	Positive Supply Voltage	+8.0 to +15V
V_{IN}	Control Input Voltage Range	0 to +5V
T_{OP}	Operating Temperature	
	(A Suffix)	-55 to +125°C
	(B Suffix)	-25 to +85°C
	(C Suffix)	0 to +70°C

ELECTRICAL CHARACTERISTICS (V– = –15V, V+ = +15V, per channel, unless otherwise noted, T_A = +25°C)

#	SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V_{ANALOG}		Analog Signal Range	-10		+10	V	
2	$r_{DS(on)}$	STATIC	Channel On Resistance		40	80	Ω	V_S = –10V
3					40	80		V_S = +2.0V
4					100	160		V_S = +10V
5	V_{IH}		Logic High Level Input Voltage	4.5	3.4		V	
6	V_{IL}		Logic Low Level Input Voltage			1.0		
7	I_{IN}		Logic Input Leakage Current		0.01	0.1	μA	V_{IN} = +5.0V
8					0.02	0.1		V_{IN} = +15V
9	$I_{D(OFF)}$		Switch OFF Leakage Current		0.2	5.0	nA	V_D = +10V, V_S = –10V
10	$I_{S(OFF)}$				0.4	5.0		V_S = +10V, V_D = –10V
11	I–		Negative Supply Quiescent Current		-2.0	-4.0	mA	V_{IN} = 0 or V+
12	I+		Positive Supply Quiescent Current		2.0	4.0		
13	t_{ON}	DYNAMIC	Switch Turn-On Time (All inputs)		150	250	nsec	V_{IN} = 5.0V
14	t_{OFF}		Switch Turn-OFF Time (All inputs)		120	220		
15	C_{CRR}		All crosstalk	62			dB	f = 10 MHz, R_L = 50Ω
16			Single Channel Crosstalk	80				
17			Frequency Roll-Off (Bandwidth)		1.0	3.0		f = 100 MHz, R_L = 50Ω
18	C_d		Output Node Capacitance		8.0	12.0	pF	V_D = 0, f = 1 MHz, V_{IN} = 0
19	C_s		Input Node Capacitance		2.5	4.0		V_S = 0

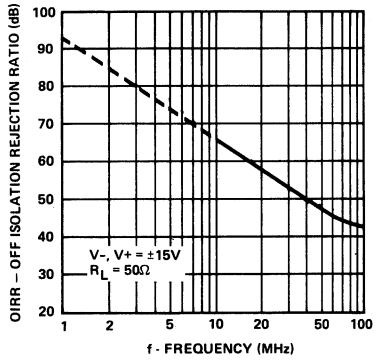
ELECTRICAL CHARACTERISTICS (V– = –15V, V+ = +15V, per channel, unless otherwise noted)

LIMITS AT TEMPERATURE EXTREMES

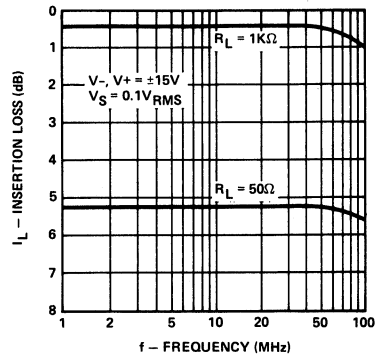
#	SYMBOL		PARAMETER	MAXIMUM @ T_A = -55°C	-25°C	+70°C	+85°C	+125°C	UNITS	TEST CONDITIONS
1	V_{ANALOG}	STATIC	Analog Signal Range	±10	±10	±10	±10	±10	V	
2	$r_{DS(on)}$		Channel On Resistance	80	80	120	120	150	Ω	V_S = –10V, I_S = -1.0 mA
3				80	80	120	120	150		V_S = +2.0V, I_S = +1.0 mA
4				160	160	240	240	300		V_S = +10V, I_S = -1.0 mA
5	I_{IN}		Logic Input	0.1	0.1	1.0	1.0	10	μA	V_{IN} = +5.0V
6			Leakage Currents	0.1	0.1	2.0	2.0	20		V_{IN} = +15V
7	$I_{D(OFF)}$		Switch OFF	5.0	5.0	100	100	1000	nA	V_D=+10V, V_S=–10V
8	$I_{S(OFF)}$		Leakage Currents	5.0	5.0	100	100	1000		V_S=+10V, V_D=–10V
9	I–		Supply	–4.0	–4.0	–4.0	–4.0	–4.0	mA	V_{IN} = 0 or V+
10	I+		Quiescent Currents	4.0	4.0	4.0	4.0	4.0		

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C, per channel, unless otherwise specified)

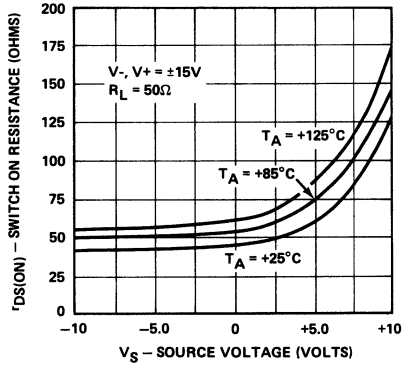
SWITCH-OFF ISOLATION REJECTION RATIO —VS— FREQUENCY



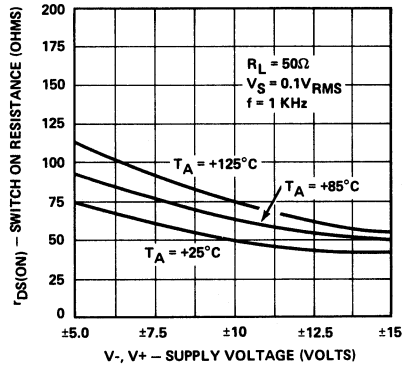
INSERTION LOSS —VS— FREQUENCY



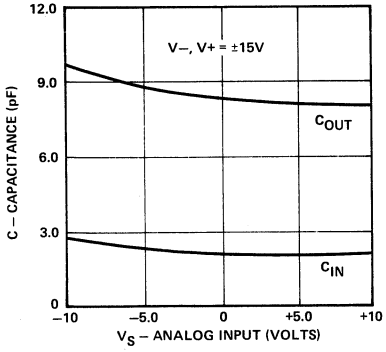
SWITCH ON RESISTANCE —VS— ANALOG VOLTAGE



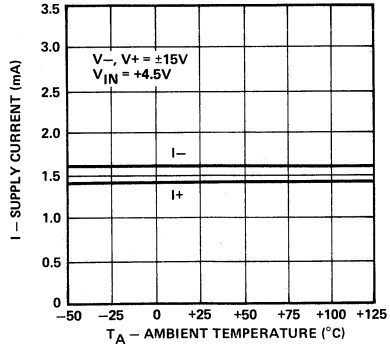
SWITCH-ON RESISTANCE —VS— SUPPLY VOLTAGES



CAPACITANCE —VS— ANALOG INPUT VOLTAGE



SUPPLY CURRENTS —VS— AMBIENT TEMPERATURE



TOPAZ SEMICONDUCTOR

CDG5341

DUAL MONOLITHIC SPST CMOS/D-MOS T-CONFIGURATION ANALOG SWITCH

ORDERING INFORMATION

Dual SPST 'T' Switch, Logic '0' OFF, Break-before-make	14-Pin Plastic DIP	14-Pin Ceramic DIP
Commercial Temp. Range	CDG5341CJ	—
Industrial Temp. Range	CDG5341BJ	CDG5341BK
Military Temp. Range	—	CDG5341AK

FEATURES

- Ultra High OFF Isolation, > 80 dB @ 10MHz
- Low Channel-to-Channel Crosstalk, > 80 dB @ 10MHz
- CMOS Compatible Inputs
- Low ON Resistance, <110Ω
- Wide Bandwidth, -1.0dB @ 50MHz

APPLICATIONS

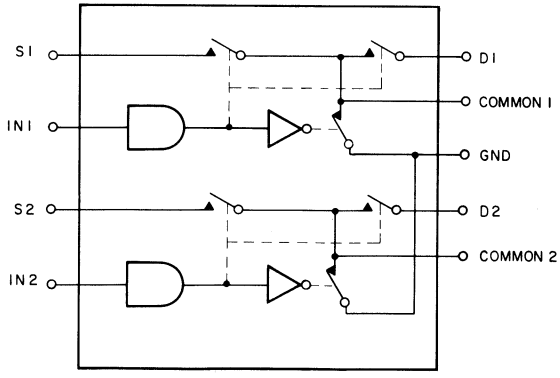
- RF & Video Switches
- Data Acquisition

DESCRIPTION

Topaz Semiconductor CMOS/D-MOS Analog Switches feature high-speed, low-power 5V CMOS input logic and level translation circuitry and high speed, low capacitance Lateral D-MOS switches. CMOS and Lateral D-MOS circuitry are fabricated together on a single silicon chip.

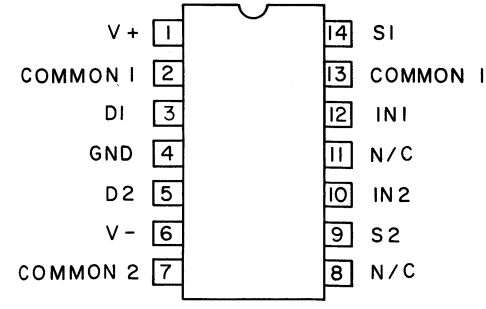
All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{cc} or GND).

FUNCTIONAL BLOCK DIAGRAM



Two SPST 'T' Switches per Package.
Switches shown in Logic '0' Input Position.
Compensation Networks can be connected to Common 1 and Common 2.

PIN CONFIGURATION



Top View

ABSOLUTE MAXIMUM RATINGS

V- Negative Supply Voltage ..... -20V
V+ Positive Supply Voltage ..... +20V
V_{IN} Control Input Voltage Range ..... V+ +0.3V, V- -0.3V

I_L Continuous Current, any Pin Except S or D ..... 20 mA
I_S Continuous Current, S or D ..... 30 mA
I_S Peak Pulsed Current, S or D, 80μsec, 1%, Duty Cycle ..... 100 mA
T_J Junction Temperature Range ..... -55 to +125°C
T_S Storage Temperature Range ..... -55 to +125°C
P_D Power Dissipation (derate at 12mW/°C, above +85°C) ..... 500 mW

RECOMMENDED OPERATING CONDITIONS

V- Negative Supply Voltage ..... -8.0 to -15V
V+ Positive Supply Voltage ..... +8.0 to +15V
V_{IN} Control Input Voltage Range ..... 0 to +5V
V_S Analog Switch Voltage Range ..... -10 to +10V
T_{OP} Operating Temperature
(A Suffix) ..... -55 to +125°C
(B Suffix) ..... -25 to +85°C
(C Suffix) ..... 0 to +70°C

ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V per channel, unless otherwise noted, T_A = +25°C)

#	SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	V_{ANALOG}	STATIC	Analog Signal Range	-10		+10	V	
2	$r_{DS(on)}$	STATIC	Switch ON Resistance		100	160	Ω	V_S = -10V, I_S = -1.0 mA
3	$r_{DS(on)}$	STATIC	Switch ON Resistance		110	160	Ω	V_S = +2.0V, I_S = +1.0 mA
4	$r_{DS(on)}$	STATIC	Switch ON Resistance		200	320	Ω	V_S = +10V, I_S = -1.0 mA
5	V_{IH}	STATIC	High Level Input Voltage	4.5	3.4		V	
6	V_{IL}	STATIC	Low Level Input Voltage			1.0	V	
7	I_{IN}	STATIC	Logic Input Leakage Current		0.01	0.1	µA	V_{IN} = +5.0V
8	I_{IN}	STATIC	Logic Input Leakage Current		0.02	0.1	µA	V_{IN} = +15V
9	$I_{D(OFF)}$	STATIC	Switch OFF Leakage Current		0.2	5.0	nA	V_D = +10V, V_S = -10V
10	$I_{S(OFF)}$	STATIC	Switch OFF Leakage Current		0.4	5.0	nA	V_S = +10V, V_D = -10V
11	I-	STATIC	Negative Supply Quiescent Current		-0.1	-0.5	µA	V_{IN} = 0 or V+
12	I+	STATIC	Positive Supply Quiescent Current		0.1	0.5	µA	V_{IN} = 0 or V+
13	t_{ON}	DYNAMIC	Switch Turn-On Time		150	250	nsec	V_{IN} = 5.0V
14	t_{OFF}	DYNAMIC	Switch Turn-OFF Time		120	220	nsec	V_{IN} = 5.0V
15	O_{IRR}	DYNAMIC	OFF Isolation, Rejection Ratio	80			dB	f = 10 MHz, R_L = 50Ω
16	C_{CRR}	DYNAMIC	Cross-Coupling Rejection Ratio	80			dB	f = 10 MHz, R_L = 50Ω
17		DYNAMIC	Frequency Roll-Off (Bandwidth)		1.0	3.0	dB	f = 50 MHz, R_L = 50Ω
18	C_d	DYNAMIC	Drain-Node Capacitance		0.3		pF	V_D = 0, f = 1MHz, V_{IN} = 0
19	C_s	DYNAMIC	Source-Node Capacitance		3.0		pF	V_S = 0, f = 1MHz, V_{IN} = 0

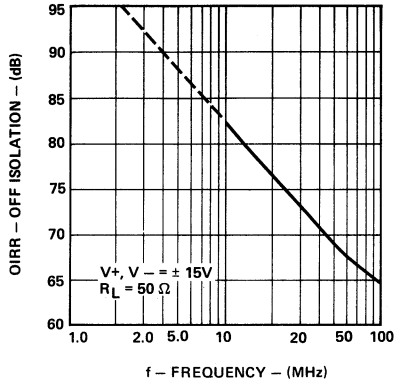
ELECTRICAL CHARACTERISTICS (V- = -15V, V+ = +15V, per channel)

LIMITS AT TEMPERATURE EXTREMES

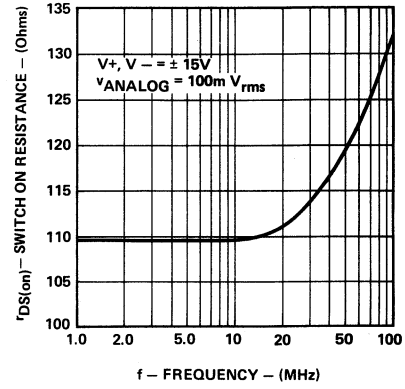
#	SYMBOL		PARAMETER	MAXIMUM @ T_A = -55°C	-25°C	70°C	+85°C	+125°C	UNITS	TEST CONDITIONS
1	V_{ANALOG}	STATIC	Analog Signal Range	±10	±10	±10	±10	±10	V	
2	$r_{DS(on)}$	STATIC	Switch On Resistance	160	160	240	240	300	Ω	V_S = -10V, I_S = -1.0 mA
3	$r_{DS(on)}$	STATIC	Switch On Resistance	160	160	240	240	300	Ω	V_S = +2.0V, I_S = +1.0 mA
4	$r_{DS(on)}$	STATIC	Switch On Resistance	320	320	480	480	600	Ω	V_S = +10V, I_S = -1.0 mA
5	I_{IN}	STATIC	Logic Input Leakage Current	0.1	0.1	1.0	1.0	10	µA	V_{IN} = +5.0V
6	I_{IN}	STATIC	Logic Input Leakage Current	0.1	0.1	2.0	2.0	20	µA	V_{IN} = +15V
7	$I_{D(OFF)}$	STATIC	Switch OFF Leakage Current	5.0	5.0	100	100	1000	nA	V_D = +10V, V_S = -10V
8	$I_{S(OFF)}$	STATIC	Switch OFF Leakage Current	5.0	5.0	100	100	1000	nA	V_S = +10V, V_D = -10V
9	I-	STATIC	Supply Quiescent Currents	-0.5	-0.5	-20	-20	-100	µA	V_{IN} = 0 or V+
10	I+	STATIC	Supply Quiescent Currents	0.5	0.5	20	20	100	µA	V_{IN} = 0 or V+

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

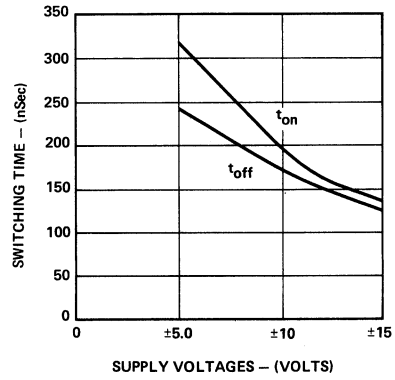
OFF ISOLATION REJECTION RATIO —VS— FREQUENCY



SWITCH ON RESISTANCE —VS— FREQUENCY



SWITCHING TIMES —VS— SUPPLY VOLTAGES



SECTION 4

DESIGN CONSIDERATIONS FOR ANALOG SWITCHES USING LATERAL D-MOS FETs

INTRODUCTION

Two Lateral D-MOS FET products recently introduced by Topaz Semiconductor, the SD211A and SD215A have maximum values of ON Resistance ($r_{DS(on)}$) specified in practical analog switch configurations. The SD211A, normally used as a +30V switch driver, also has applications as a ±5V analog switch.

CONFIGURATION

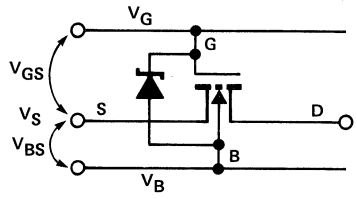


Figure 1

MAXIMUM VOLTAGES

DEVICE	VS(1) ANALOG INPUT VOLTAGE RANGE	VG(2) CONTROL INPUT VOLTAGE RANGE	VB(3) BODY VOLT.
SD211A	-5.0V to +5.0V	-10V to +15V	-10V
SD215A	-10V to +10V	-15V to +15V	-15V

(1) Maximum range of Analog Input Voltage (V_s) is limited by the Source-Drain Breakdown Voltage (BV_{SD}) of the D-MOS FET. If the breakdown voltage is exceeded the analog switch will have high OFF Leakage.

(2) Control Input Voltage (V_G) must be set so that it turns the D-MOS FET OFF with the Analog Input (V_s) at the most negative voltage and ON at the most positive Analog Input voltage.

(3) As a minimum, Body Bias Voltage (V_B) is set to the most negative point in the circuit to prevent the Gate protective diode or internal device diodes being forward biased under any condition of applied voltages. In practice V_B should remain negative with respect to V_S to avoid excessive increases in Source-to-Body Capacitance.

DESIGN CONSIDERATIONS

The ON Resistance ($r_{DS(on)}$) of the D-MOS FET depends upon the Gate-Source Voltage (V_{GS}) added to Threshold Voltage ($V_{GS(th)}$) of the FET. The lowest or least voltage added to Threshold Voltage or highest ON Resistance is when the analog input is at the most positive value. The following curve illustrates ON Resistance change as a function of Analog Input Voltage:

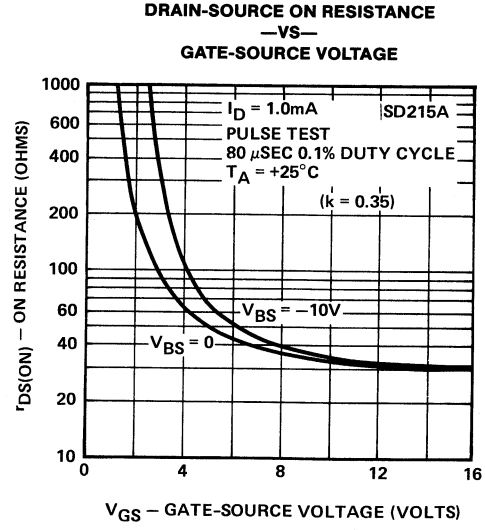


Figure 2

GAMMA EFFECT

The actual Threshold Voltage in an analog switch configuration is higher than the value on the data sheet because of the effect of Body-Source Voltage (V_{BS}). The following curve illustrates change in Threshold Voltage as a function of Body to Source Bias Voltage:

DESIGN CONSIDERATIONS FOR ANALOG SWITCHES USING LATERAL D-MOS FETs (continued)

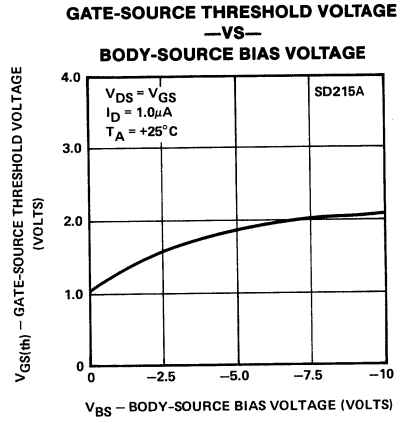


Figure 3

The change or increase in Threshold Voltage with Body to Source Bias Voltage applied is described by the following equation:

$$V_{GS(th)1} = V_{GS(th)0} + k\sqrt{|V_{BS}|}$$

The "k factor" or Gamma controls the increase in Threshold Voltage or "Up Threshold" with Body Voltage. $V_{GS(th)}$ also changes with temperature as shown on the following curve:

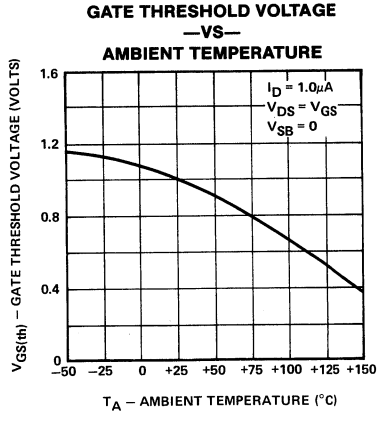


Figure 4

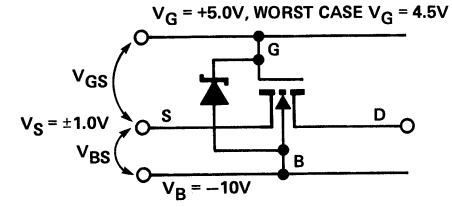
CONCLUSION

Low Gamma D-MOS FETs from Topaz Semiconductor offer design solutions for low Gate Drive Voltage Analog Switches.

DESIGN EXAMPLE:

Use an SD215A to switch a ±1.0 Volt signal in a 5.0 Volt system. Compare test results to those obtained with a competitor's SD215.

CONFIGURATION



$V_{GS(on)}$ = +3.5V min., V_{BS} = -11V

$$V_{GS(th)1} = V_{GS(th)0} + k\sqrt{|V_{BS}|} \quad (1)$$

$$r_{DS(on)} = \frac{1}{K(V_{GS(on)} - V_{GS(th)1})} \quad (2)$$

Note: K is the Device Constant, $K \approx \frac{W\mu\ Co}{L}$

for this type of Lateral D-MOS, K ≈ .003

TEST RESULTS

1. Topaz SD215A, (k = 0.35)

$V_{GS(th)0}$	$V_{GS(th)1}$	$r_{DS(on)}$
0.75V	1.91V	209 ohms
1.00V	2.16V	248 ohms
1.25V	2.41V	305 ohms
1.50V	2.66V	396 ohms

2. Competitor's SD215, (k = 0.65)

$V_{GS(th)0}$	$V_{GS(th)1}$	$r_{DS(on)}$
0.75V	2.90V	555 ohms
1.00V	3.15V	952 ohms
1.25V	3.40V	3300 ohms
1.50V	3.65V	OFF

DESIGN CONSIDERATIONS FOR THE CDG4469J DIGITAL CONTROLLED ATTENUATOR

INTRODUCTION

Conventional methods of controlling amplifier gain such as change of device transconductance or by resistor divider networks can result in unwanted phase shift or loss of bandwidth.

Typical low frequency gain control circuits involve changing gain setting resistors which causes changes in offset and, when compensated, adds unwanted phase shift. To minimize both effects the gain setting resistors will have to be of low value.

In high frequency applications a lot of extra circuitry is required to compensate and stabilize circuits. Here gain control is done mostly by varying the transconductance of individual gain stages. The result is a change from the optimum operating point to one that is less desirable. The side effects are an increase in noise, loss of bandwidth, shift in input and output impedance and unwanted phase shift. In narrow band amplifiers this causes mismatch to filters and the degradation of in-band frequency components.

The CDG4469J Digital Controlled Attenuator meets the need for an attenuation concept that overcomes these problems and provides gain control over a wide dynamic range. The CDG4469 allows gain control over a range of 127.5dB in 0.5dB steps via an 8-bit digital parallel control port over a wide frequency range with constant input and output impedance. Since the CDG4469 input and output ports are strictly resistive, the device can be placed directly in a DC path. This capability is very useful when controlling the gain of an amplifier by the feedback loop.

GAIN CONTROL CIRCUITS

Figure 1 shows a circuit for the CDG4469J used in a high frequency gain control application.

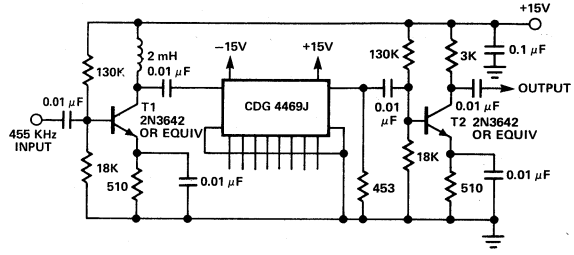


Figure 1

The circuit uses an NPN transistor biased at the optimum operating point with an RF choke as the DC pass for the collector. The CDG4469 is AC coupled to the collector of T1 and becomes the effective load of that gain stage. The output of the CDG4469 is then coupled to the input of the next gain stage, T2 and sees an AC load of 453 ohms. Gain can then be digital controlled with no effect on the transfer characteristic.

An amplifier gain control circuit which includes a band pass filter, where matching is critical, is shown in figure 2:

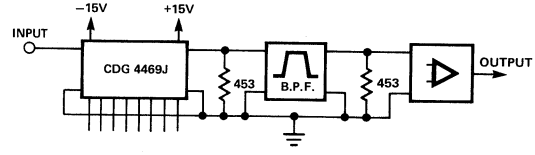


Figure 2

In this circuit the CDG4469 Attenuator can be placed either in front or after the filter. A change in gain of the Attenuator will have no effect on the band-pass characteristic because input and output impedances of the attenuator are constant. Since the CDG4469 can handle large signals and has the noise voltage characteristic of a 600 ohm resistor, it can be placed in the circuit directly in front of the amplifier.

DESIGN CONSIDERATIONS FOR THE CDG4469J DIGITAL CONTROLLED ATTENUATOR (continued)

A circuit which controls gain by controlling the amount of feedback is shown in Figure 3:

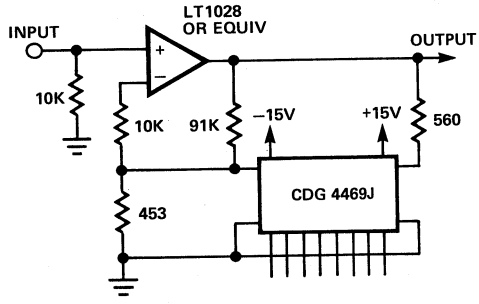


Figure 3

In the above circuit the CDG4469 is an excellent choice because of wide bandwidth, low phase shift and constant input and output impedance. Placing a resistor across the attenuator limits the maximum gain and leaves the amplifier in a controlled operating range.

Should there be a need for attenuation only, the CDG4469 can be placed directly in the signal path of an amplifier as shown in Figure 4:

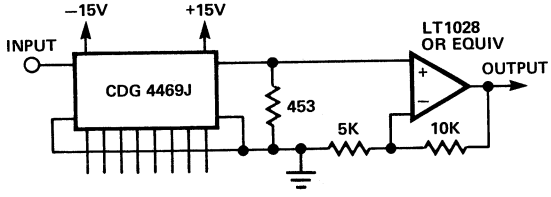


Figure 4

As indicated above, the added noise voltage from the CDG4469 is equal to that of a 600 ohm resistor and is constant over the entire attenuation control range.

DISTORTION COMPENSATION CIRCUIT

An attenuator/amplifier circuit which uses power supply modulation to minimize total harmonic distortion is shown in Figure 5:

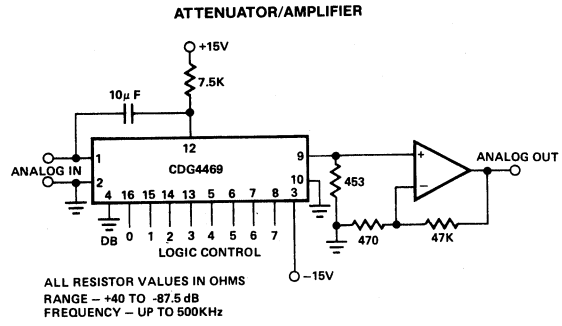


Figure 5

In the above circuit a portion of the analog input is added to the positive supply voltage because the 7.5K ohm resistor in series with the supply and the 650 ohm input resistor form a voltage divider network. This modulates the ON resistance of the internal FET switches to maintain constant insertion loss over the analog voltage input range. The 10μF capacitor used gives a low frequency corner of about 20 Hz.

ATTENUATOR CHARACTERIZATION

Figures 6, 7 and 8 show total harmonic distortion characteristics as a function of attenuation setting and level of analog input. The compensation circuit is the same as illustrated in Figure 5 above.

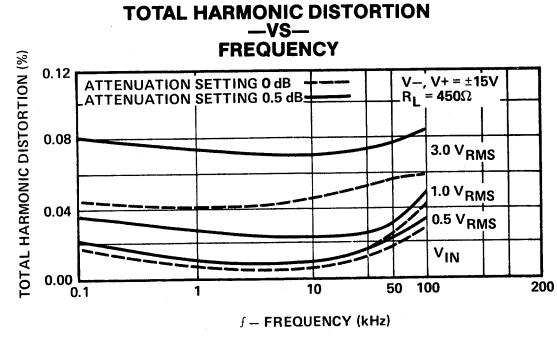


Figure 6

DESIGN CONSIDERATIONS FOR THE CDG4469J DIGITAL CONTROLLED ATTENUATOR (continued)

TOTAL HARMONIC DISTORTION —VS— FREQUENCY

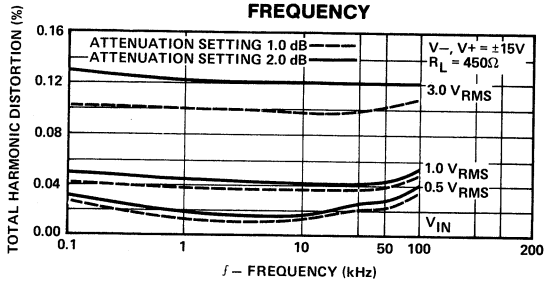


Figure 7

TOTAL HARMONIC DISTORTION —VS— FREQUENCY

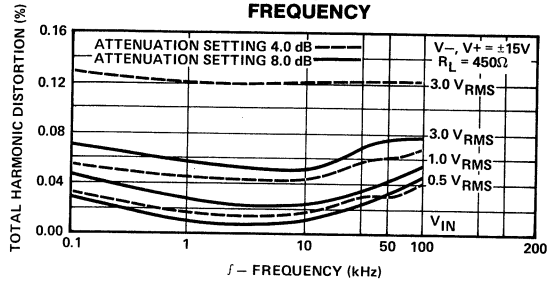


Figure 8

Figure 9 shows attenuation change -vs- attenuation setting -vs- ambient temperature. All attenuation changes are referenced to 0dB at an ambient temperature of +25°C.

ATTENUATION CHANGE —VS— ATTENUATION SETTING —VS— AMBIENT TEMPERATURE

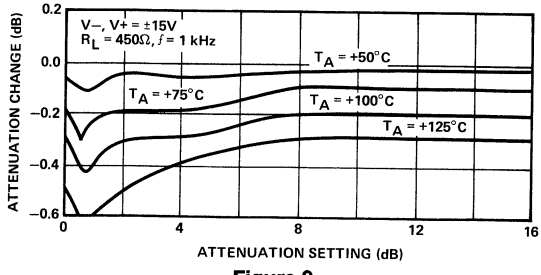


Figure 9

Figure 10 shows phase shift characteristics as a function of attenuation setting and logarithmic change in frequency.

PHASE ANGLE —VS— FREQUENCY —VS— ATTENUATION SETTING

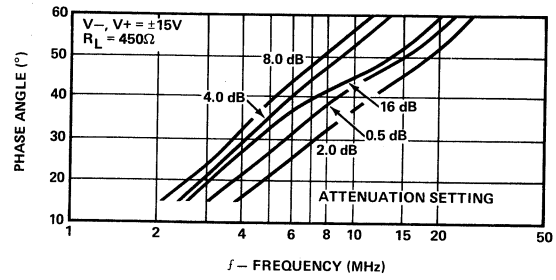


Figure 10

OTHER DESIGN CONSIDERATIONS

Analog input ground (pin 2) and analog output ground (pin 10) must be connected to a common point. Logic control ground (pin 4) is separate from analog ground.

The CDG4469 can be placed at the optimum point in any circuit and be controlled by a digital line. With latches added in front of the control inputs the CDG4469 attenuation settings can be retained until it is necessary to update them. This concept is very useful when the CDG4469 is controlled by a computer.

If attenuation steps of less than 0.5dB are required two CDG4469's can be connected in parallel. With two attenuators in parallel attenuation is 0.25dB per step and the total attenuation range is 63.75dB.

CONCLUSION

The CDG4469 attenuator with constant input and output impedance regardless of attenuation setting is adding new dimensions to the design of gain controlled amplifiers. The CDG4469 attenuation accuracy is maintained up to about 500KHz with full attenuation range and up to 5.0MHz with 6 bits or 31.5dB of attenuation range.

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